DATA SHEET

旭曜科技 ORISE TECH

OTM3225A

720-channel 6-bit source driver and 320-channel gate driver with System-On-Chip (SOC) for color amorphous TFT LCD

Preliminary

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Version 0.1

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1. GENERAL DESCRIPTION

The OTM3225A, a 262144-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 240xRGBx320 in resolution which can be achieved by the designated RAM for graphic data. The 720-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter.

The OTM3225A is able to operate with low IO interface power supply up to 1.65V and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

The built-in timing controller in OTM3225A can support several interfaces for the diverse request of medium or small size portable display. OTM3225A provides system interfaces, which include 8-/9-/16-/18-bit parallel interfaces and serial interface (SPI), to configure system. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. In addition, the OTM3225A incorporates 6, 8, 16, and 18-bit RGB interfaces for picture movement display. The OTM3225A also supports a function to display eight colors and a standby mode for power control consideration.

2. FEATURE

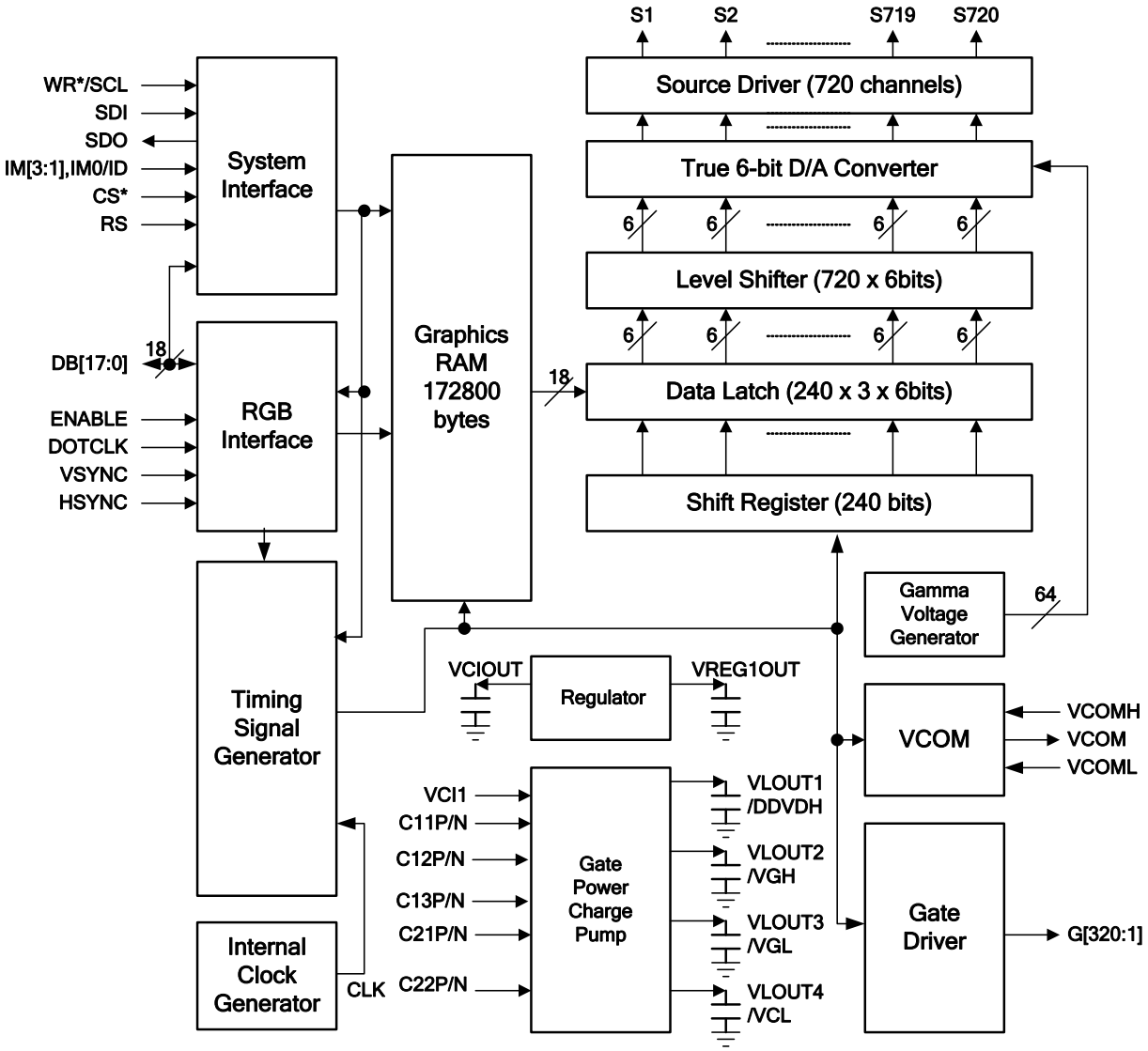
- One-chip solution for amorphous TFT-LCD.
- Supports resolution up to 240xRGBx320, incorporating a 720-channel source driver and a 320-channel gate driver
- Outputs 64 γ -corrected values using an internal true 6-bit resolution D/A converter to achieve 262K colors
- Built-in 172800 bytes internal RAM
- Line Inversion AC drive / frame inversion AC drive
- System interfaces
  - Intel 80-system with 8-, 9-, 16-, and 18-bit parallel ports
  - Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - 6-, 8-, 16-, and 18-bit RGB interfaces
- Diverse RAM accessing for functional display
  - Window address function to display at any area on the screen via a moving picture display interface
  - Window address function to limit the data rewriting area and reduce data transfer
  - Moving and still picture can display at the same time
  - Vertical scrolling function
  - Partial screen display
- Power supply
  - I/O interface supply voltage (IOVCC): 1.65 ~ 3.3 V
  - Analog power supply voltage (VCI): 2.5 ~ 3.3 V
- Resize function(x 1/2, x 1/4)
- On-chip power management system
  - Power saving mode (standby / 8-color mode, etc)
  - Low power consumption structure for source driver.
- Built-in Charge Pump circuits
  - Source driver voltage level: DDVDH-GND=4.5V ~ 6V.
  - Gate driver voltage level (VGH, VGL)
    VGH = 10.0V ~20.0V
    VGL = -4.5V ~ -13.5V
    VGH – VGL < 30.0V
  - Built-in internal oscillator and hardware reset

3. ORDERING INFORMATION

Product Number	Package Type
OTM3225A-C3	Chip Form with Gold Bump

4. BLOCK DIAGRAM

4.1. Block Function



4.2. System Interface

4.2.1. Interface

The OTM3225A supports two kind of system interfaces :

1. Intel 80-system interfaces with 8-, 9-, 16-, 18-bits parallel port.
2. Serial Peripheral Interface (SPI).

The OTM3225A has a 16-bit index register (IR) and two 18-bit data registers, a write-data register (WDR) and a read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM or control register.

When graphic data is written to the internal GRAM from MCU's graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is read via the RDR from the internal GRAM. Therefore, invalid data is first read out to the data bus when the OTM3225A executes the 1st read operation. Thus, valid data can be read out after the OTM3225A executes the 2nd read operation.

4.2.2. External Display Interface

The OTM3225A supports external RGB interface for picture movement display.

The OTM3225A allows switching between one of the external display interfaces and the system interface via pin configuration so that the optimum interface is selected for still / moving picture displayed on the screen.

When the RGB interface is chosen, display operations are synchronized with external supplied signals, VSYNC, HSYNC, and DOTCLK. Moreover, valid display data (DB17-0) is written to GRAM, which synchronized with signal (DE) enabling.

4.2.3. Address Counter (AC)

OTM3225A features an Address Counter (AC) giving an address to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

4.2.4. Graphics RAM (GRAM)

OTM3225A features a 172800-byte (240 x 320 x 18 / 8) Graphic RAM (GRAM).

4.2.5. Grayscale Voltage Generating Circuit

OTM3225A has true 6-bit resolution D/A converter, which generates 64 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register.

4.2.6. Timing Controller

OTM3225A has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, RAM accessing timing, etc.

4.2.7. Oscillator (OSC)

The OTM3225A also features an internal oscillator to generate RC oscillation with an internal resistor. In standby mode, RC oscillation is halted to reduce power consumption.

4.2.8. Source Driver Circuit

OTM3225A consists of a 720-output source driver circuit (S1 ~ S720). Data in the GRAM are latched when the 720th bit data is input. The latched data controls the source driver and generates a drive waveform.

4.2.9. Gate Driver Circuit

OTM3225A consists of a 320-output gate driver circuit (G1~G320). The gate driver circuit outputs gate driver signals at either VGH or VGL level.

4.2.10. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels DDVDH, VGH, VGL and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

5. SIGNAL DESCRIPTIONS

<table>
<tr><th>Signal</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td colspan="4">System Configuration Input Signal</td></tr>
<tr><td>IM3~1, IM0/ID</td><td>I</td><td>GND/ IOVCC</td><td>Select an interface mode to MPU.
In serial interface operation, the IM0 pin is used to set the ID bit of device code.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ I D</th><th>Interface Mode</th><th>DB Pin</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td><td>262,144 or 65,536</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td><td>262,144 or 65,536</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>*(ID)</td><td>Clock synchronous serial interface</td><td>-</td><td>262,144 or 65,536</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td><td>262,144 only</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td><td>262,144 only</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
</table></td></tr>
<tr><td>/RESET</td><td>I</td><td>MPU</td><td>RESET pin. This is an active low signal.</td></tr>
<tr><td colspan="4">Interface input Signals</td></tr>
<tr><td>/CS</td><td>I</td><td>MPU</td><td>Chip select signal.
Low: the OTM3225A is accessible.
High: the OTM3225A is not accessible.
Must connect to the IOVCC level when not used.</td></tr>
<tr><td>RS</td><td>I</td><td>MPU</td><td>Register select signal.
Low: Index register or internal status is selected.
High: Control register is selected.
Must connect to the GND or IOVCC level when not used.</td></tr>
<tr><td>(/WR) / (SCL)</td><td>I</td><td>MPU</td><td>(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low.
(B) In SPI mode, served as a synchronizing clock signal.</td></tr>
<tr><td>/RD</td><td>I</td><td>MPU</td><td>In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low.
Must connect to the GND or IOVCC level when not in use.</td></tr>
<tr><td>SDI</td><td>I</td><td>MPU</td><td>Series Data is the input on the rising edge of the SCL signal in SPI mode.
Must connect to the GND or IOVCC level when not in use.</td></tr>
<tr><td>SDO</td><td>O</td><td>MPU</td><td>Series Data is the output on the rising edge of the SCL signal in SPI mode.
Must keep this pin open(floating) when not used.
Can not connect to the GND or IOVCC level when not in use.</td></tr>
</table>

<table>
<tr><th>Signal</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td>DB0-DB17</td><td>I/O</td><td>MPU</td><td>Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table:
<table>
<tr><th>Mode</th><th>Pin Assignment</th></tr>
<tr><td>8-bit system interface</td><td>DB17-DB10</td></tr>
<tr><td>9-bit system interface</td><td>DB17-DB9</td></tr>
<tr><td>16-bit system interface</td><td>DB17-DB10, DB8-DB1</td></tr>
<tr><td>18-bit system interface</td><td>DB17-DB0</td></tr>
<tr><td>6-bit External (RGB) interface</td><td>DB17-DB12</td></tr>
<tr><td>8-bit External (RGB) interface</td><td>DB17-DB10</td></tr>
<tr><td>16-bit External (RGB) interface</td><td>DB17-13, DB11-DB1</td></tr>
<tr><td>18-bit External (RGB) interface</td><td>DB17-DB0</td></tr>
<tr><td>Serial interface(SPI)</td><td>Not use</td></tr>
</table>
Must connect to the GND or IOVCC level when not in use.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>MPU</td><td>In external RGB interface mode, served as a vertical synchronize signal input
Must connect to the IOVCC or GND level when not in use.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>MPU</td><td>In external RGB interface mode, served as a horizontal synchronized signal input
Must connect to the IOVCC or GND level when not used.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>MPU</td><td>In external RGB interface mode, polarity of ENABLE signal is synchronized with valid graphic data input.
Low: Valid data on DB17-DB0 (relative to different interface modes)
High: Invalid data on DB17-DB0 (relative to different interface modes)
Moreover, setting EPL bit can change the polarity of the ENABLE signal.
Must connect to the GND or IOVCC level when not in use.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>MPU</td><td>In external RGB interface mode, served as a dot clock signal.
When DPL = “0”: Input data on the rising edge of DOTCLK
When DPL = “1”: Input data on the falling edge of DOTCLK
It is fixed to the IOVCC or GND level when not in use.</td></tr>
<tr><td>FMARK</td><td>O</td><td>MPU</td><td>Frame head pulse signal, which is used when writing data to the internal RAM.
Must keep this pin open(floating) when not used.
Can not connect to the GND or IOVCC level when not in use.</td></tr>
<tr><td colspan="4">Charge Pump and Power Supply Signal</td></tr>
<tr><td>C11P/N,
C12P/N
C13P/N
C21P/N,
C22P/N</td><td>-</td><td>Step-up capacitor</td><td>Connect boost capacitors for the internal DC/DC converter circuit to these pins.</td></tr>
<tr><td>VCI1</td><td>I/O</td><td>Stabilizing capacitor</td><td>Reference voltage of step-up circuit 1. Make sure the output voltage levels from DDVDH, VGH, and VGL do not exceed the respective setting ranges.</td></tr>
<tr><td>DDVDH</td><td>I</td><td>Stabilizing capacitor</td><td>Power supply for the source driver liquid crystal drive unit and VCOM drive. DDVDH = 4.5V ~ 6.0V</td></tr>
<tr><td>VGH</td><td>I</td><td>Stabilizing capacitor</td><td>Liquid crystal drive power supply.</td></tr>
<tr><td>VGL</td><td>I</td><td>Stabilizing capacitor</td><td>Liquid crystal drive power supply.</td></tr>
<tr><td>VCL</td><td>O</td><td>Stabilizing</td><td>VCOML drive power supply. Make sure to connect to stabilizing capacitor. VCL = -1.9V ~</td></tr>
</table>

Signal	I/O	Connected with	Function
		capacitor	-3.0V
VPP2	I	Power supply or open	Power supply for OTP programming.
Source/Gate Driver and VCOM Signals			
G1~G320	O	LCD	Output gate driver signals, which has the swing from VGH to VGL
S1~S720	O	LCD	Output source driver signals. The D/A converted 64-gray-scale analog voltage is output.
VREG1OUT	O	Stabilizing capacitor	Output voltage generated from the reference voltage (VCI or VCIR). The factor is determined by instruction (VRH bits). VREG1OUT is used for : (1) source driver grayscale reference voltage (2) VCOMH level reference voltage (3) VCOM amplitude reference voltage Connect to a stabilizing capacitor when in use. VREG1OUT = 4.0V ~ (DDVDH – 0.5)V
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register. Also, the VCOM output can be started and halted by register setting.
VCOMH	O	Stabilizing capacitor	The High level of VCOM amplitude. The output level can be adjusted by electronic volume. Make sure to connect to stabilizing capacitor.
VCOML	O	Stabilizing capacitor	The Low level of VCOM amplitude. The output level can be adjusted by instruction (VDV bits). VCOML = (VCL+0.5) V ~ 0V. Make sure to connect to stabilizing capacitor.
VGS	I	GND	Reference level for the grayscale voltage generating circuit.
GND	P	Power supply	Internal logic GND: GND = 0V.
RGND	P	Power supply	Internal RAM GND. RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.
VDDD	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.
IOVCC	P	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVCC = 1.65V ~ 3.3V. Note: Must keep VCI ≥IOVCC.
AGND	P	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VCI	P	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.
Misc. Signal			
IOGNDDUM	I/O	Open	Test pins. Leave them open.
DUMMY1~15 DUMMY20~27	I/O	Open	Test pins. Leave them open.
TESTO2~16	I/O	Open	Test pins. Leave them open.
TEST1~3	I/O	Open	Test pins. Leave them open.
TS0~8	I/O	Open	Test pins. Leave them open

6. INSTRUCTIONS

6.1. Outline

The OTM3225A supports 18-bit data bus interface to access command register to configure system. When the command register accessing is desired, sending the command information to specify which index register would be accessed and following the data to that control register. Moreover, register accessing operation should cooperate with RS, /WR, /RD signal for OTM3225A to recognize the control instruction. And command instruction can be accomplished by using all system interfaces (18-bit, 16-bit, 9-bit, 8-bit 80 system and SPI). The corresponding pin assignment of different system interface are shown in Figure 6-1 to Figure 6-5

The instruction can be categorized into 8 groups. And the 8 groups are:

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ-correction

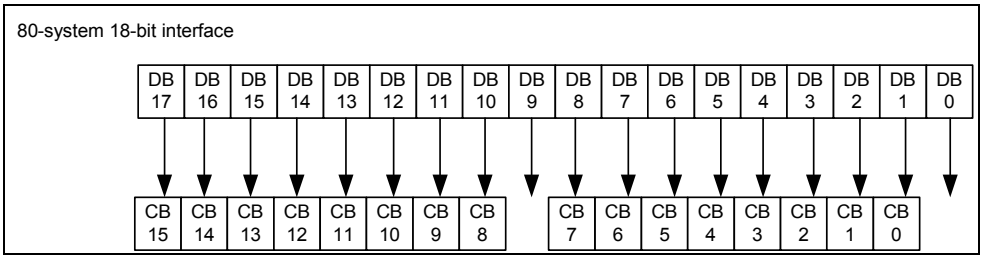


Figure 6-1 : I80-system 18bits interface data transfer format

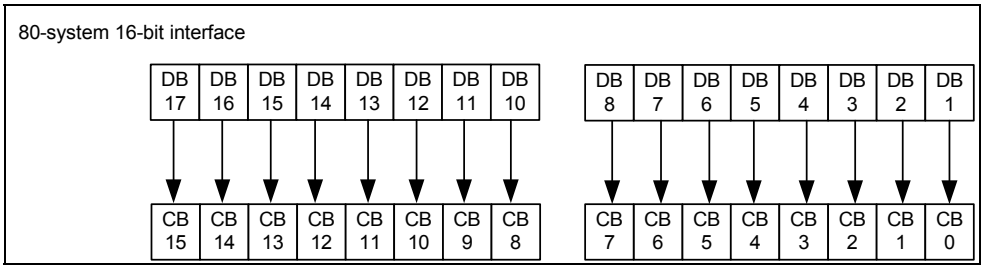


Figure 6-2 : I80-system 16bits interface data transfer format

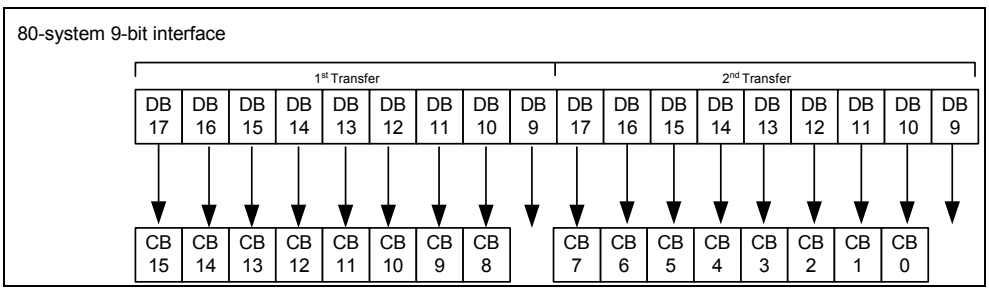


Figure 6-3 : I80-system 9bits interface data transfer format

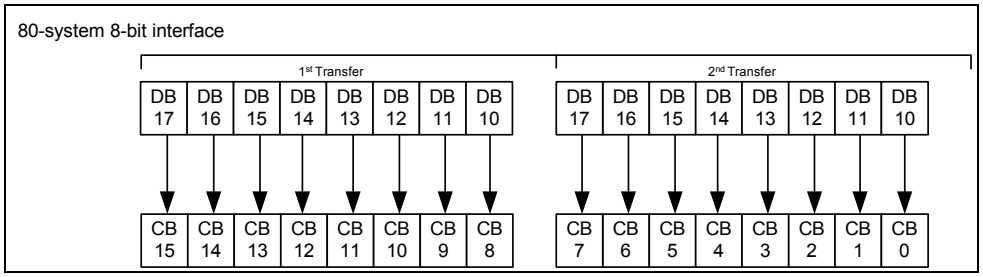


Figure 6-4 : I80 8bits interface data transfer format

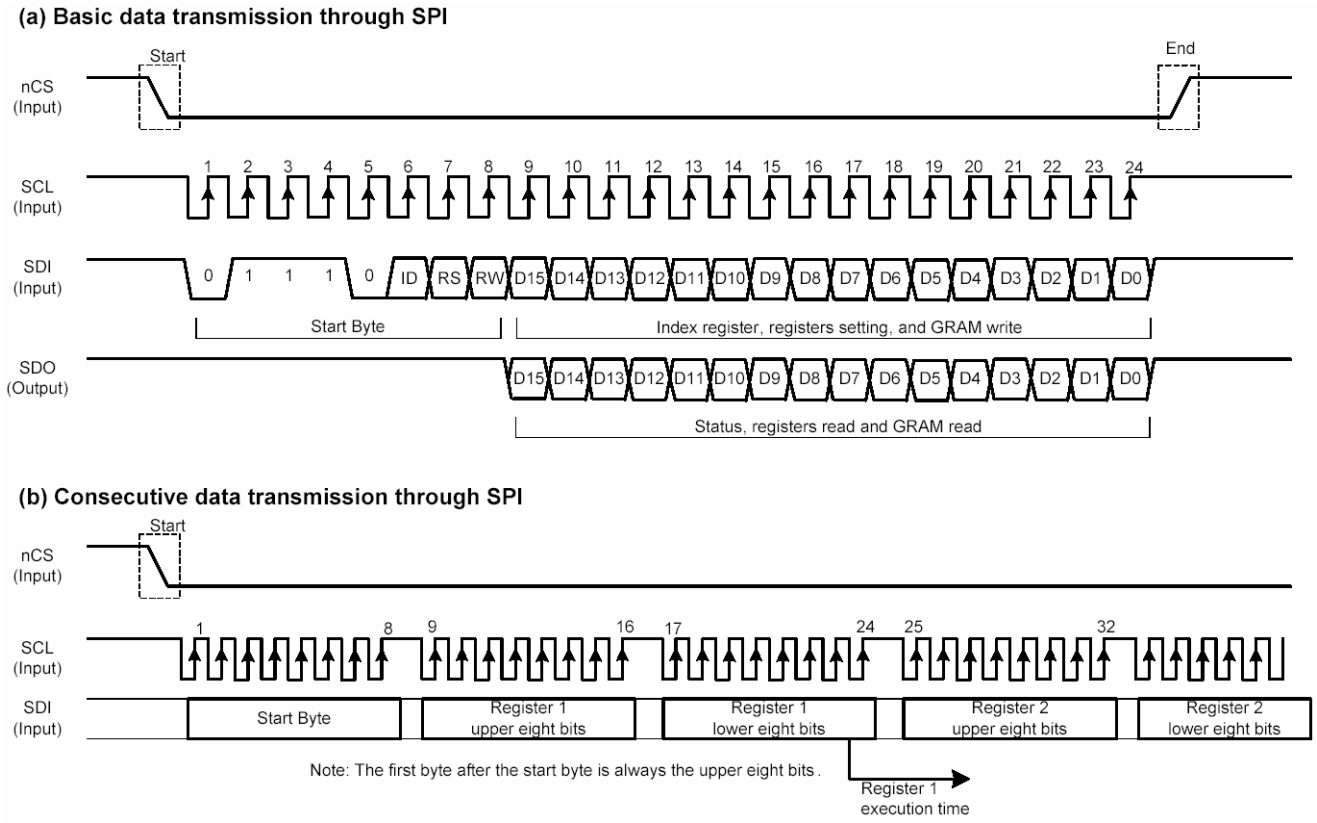


Figure 6-5 : Serial interface data transfer format

6.2. Instruction

Table 6-1 Instruction List Table

Register No	Register	Upper 8-bit								Lower 8-bit							
		CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
00h	ID Read	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
01h	Driver Output Control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0
02h	LCD Drive Waveform Control	0	0	0	0	0	1	B/C (0)	EOR (0)	0	0	0	0	0	0	0	0
03h	Entry Mode	TRIREG (0)	DFM (0)	0	BGR (0)	0	0	0	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	0	0
04h	Scaling Control	0	0	0	0	0	0	RCV1 (0)	RCV0 (0)	0	0	RCH1 (0)	RCH0 (0)	0	0	RSZ1 (0)	RSZ0 (0)
07h	Display Control (1)	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	0	GON (0)	DTE (0)	CL (0)	0	D1 (0)	D0 (0)
08h	Display Control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
09h	Display Control (3)	0	0	0	0	0	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (1)	ISC0 (1)
0Ah	Frame Cycle Control	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE (0)	FMI2 (0)	FMI1 (0)	FMI0 (0)
0Ch	External Display interface control (1)	0	ENC2 (0)	ENC1 (0)	ENC0 (0)	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
0Dh	Frame Maker Position	0	0	0	0	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)
0Fh	External Display interface control (2)	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)
10h	Power Control (1)	0	0	0	SAP (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	AP2 (1)	AP1 (0)	AP0 (0)	0	0	SLP (0)	STB (0)
11h	Power Control (2)	0	0	0	0	0	DC12 (1)	DC11 (1)	DC10 (1)	0	DC02 (1)	DC01 (1)	DC00 (1)	0	VC2 (0)	VC1 (0)	VC0 (0)
12h	Power Control (3)	0	0	0	0	0	0	0	0	VCIRE (0)	0	0	1	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)
13h	Power Control (4)	0	0	0	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0
20h	GRAM address Set Horizontal Address	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
21h	GRAM address Set Vertical Address	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)
22h	Write Data to GRAM Read Data from GRAM																
29h	Power Control (7)	0	0	0	0	0	0	0	0	0	0	0	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)
2Bh	Frame Rate Control	0	0	0	0	0	0	0	0	0	0	0	0	FRS3 (1)	FRS2 (0)	FRS1 (1)	FRS0 (1)
30h	γ Control (1)	0	0	0	0	0	KP1[2] (0)	KP1[1] (0)	KP1[0] (0)	0	0	0	0	0	KP0[2] (1)	KP0[1] (0)	KP0[0] (0)
31h	γ Control (2)	0	0	0	0	0	KP3[2] (0)	KP3[1] (1)	KP3[0] (1)	0	0	0	0	0	KP2[2] (1)	KP2[1] (1)	KP2[0] (0)
32h	γ Control (3)	0	0	0	0	0	KP5[2] (0)	KP5[1] (0)	KP5[0] (0)	0	0	0	0	0	KP4[2] (0)	KP4[1] (1)	KP4[0] (1)
35h	γ Control (4)	0	0	0	0	0	RP1[2] (0)	RP1[2] (1)	RP1[0] (1)	0	0	0	0	0	RP0[2] (0)	RP0[2] (1)	RP0[0] (1)
36h	γ Control (5)	0	0	0	VRP1[4] (0)	VRP1[3] (1)	VRP1[2 (1)]	VRP1[1] (1)	VRP1[0] (0)	0	0	0	VRP0[4] (0)	VRP0[3] (0)	VRP0[2] (1)	VRP0[1] (1)	VRP0[0] (0)
37h	γ Control (6)	0	0	0	0	0	KN1[2] (1)	KN1[1] (0)	KN1[0] (0)	0	0	0	0	0	KN0[2] (1)	KN0[1] (1)	KN0[0] (1)
38h	γ Control (7)	0	0	0	0	0	KN3[2] (0)	KN3[1] (0)	KN3[0] (1)	0	0	0	0	0	KN2[2] (1)	KN2[1] (0)	KN2[0] (0)
39h	γ Control (8)	0	0	0	0	0	KN5[2] (0)	KN5[1] (1)	KN5[0] (1)	0	0	0	0	0	KN4[2] (1)	KN4[1] (1)	KN4[0] (1)
3Ch	γ Control (9)	0	0	0	0	0	RN1[2] (0)	RN1[1] (1)	RN1[0] (1)	0	0	0	0	0	RN0[2] (0)	RN0[1] (1)	RN0[0] (10)
3Dh	γ Control (10)	0	0	0	VRN1[4] (0)	VRN1[3] (0)	VRN1[2] (1)	VRN1[1] (0)	VRN1[0] (0)	0	0	0	VRN0[4] (0)	VRN0[3] (1)	VRN0[2] (0)	VRN0[1] (1)	VRN0[0] (1)
50h	Window Horizontal RAM Address Start	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
51h	Window Horizontal RAM Address End	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
52h	Window Vertical RAM Address Start	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
53h	Window Vertical RAM Address End	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)
60h	Driver Output Control	GS (0)	0	NL5 (1)	NL4 (0)	NL3 (0)	NL2 (1)	NL1 (1)	NL0 (1)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
61h	Driver Output Control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)
6Ah	Vertical Scroll Control	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
80h	Display Position - Partial Display 1	0	0	0	0	0	0	0	PTDP08 (0)	PTDP07 (0)	PTDP06 (0)	PTDP05 (0)	PTDP04 (0)	PTDP03 (0)	PTDP02 (0)	PTDP01 (0)	PTDP00 (0)
81h	RAM Address Start - Partial Display 1	0	0	0	0	0	0	0	PTSA08 (0)	PTSA07 (0)	PTSA06 (0)	PTSA05 (0)	PTSA04 (0)	PTSA03 (0)	PTSA02 (0)	PTSA01 (0)	PTSA00 (0)
82h	RAM Address End - Partial Display 1	0	0	0	0	0	0	0	PTEA08 (0)	PTEA07 (0)	PTEA06 (0)	PTEA05 (0)	PTEA04 (0)	PTEA03 (0)	PTEA02 (0)	PTEA01 (0)	PTEA00 (0)
83h	Display Position - Partial Display 2	0	0	0	0	0	0	0	PTDP18 (0)	PTDP17 (0)	PTDP16 (0)	PTDP15 (0)	PTDP14 (0)	PTDP13 (0)	PTDP12 (0)	PTDP11 (0)	PTDP10 (0)

84h	RAM Address Start - Partial Display 2	0	0	0	0	0	0	0	PTSA18 (0)	PTSA17 (0)	PTSA16 (0)	PTSA15 (0)	PTSA14 (0)	PTSA13 (0)	PTSA12 (0)	PTSA11 (0)	PTSA10 (0)
85h	RAM Address End - Partial Display 2	0	0	0	0	0	0	0	PTEA18 (0)	PTEA17 (0)	PTEA16 (0)	PTEA15 (0)	PTEA14 (0)	PTEA13 (0)	PTEA12 (0)	PTEA11 (0)	PTEA10 (0)
90h	Panel interface Control 1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (0)	RTNI1 (0)	RTNI0 (0)
92h	Panel Interface Control 2	0	0	0	0	0	NOWI2 (1)	NOWI1 (1)	NOWI0 (0)	0	0	0	0	0	0	0	0
95h	Panel Interface Control 4	0	0	0	0	0	0	DIVE1 (1)	DIVE0 (0)	0	0	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)
97h	Panel Interface Control 5	0	0	0	0	NOWE3 (1)	NOWE2 (1)	NOWE1 (0)	NOWE0 (0)	0	0	0	0	0	0	0	0

The following are detailed explanations of instructions with illustrations of instruction bits (CB15-0) assigned to each interface.

6.2.1. Index Register (IR)

R/W	RS	CB15	CCB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h ~ RFFh) of a control register or RAM. The index range is from “0000_0000” to “1111_1111” in binary format.

6.2.2. ID Read Register (SR)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

The IC code of OTM3225A can be accessed by read operation. The 16-bits ID Code can be read out when read ID operation is executed. The ID information can be set from 0x0000h to 0xFFFFh by IC metal option for customer’s request.

6.2.3. Driver Output Control Register (R01h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0

SS: Shift direction of the source driver output selection.

When SS = “0”, source driver shift from S1 to S720.

When SS =“1”, source driver shift from S720 to S1. Moreover, SS can cooperate with BGR for different color filter configuration of LCD panel. The combination of SS and BGR bit are summarized at **Table 6-2**.

★**Note:** After changing SS bit or BGR bit, display data must be rewritten.

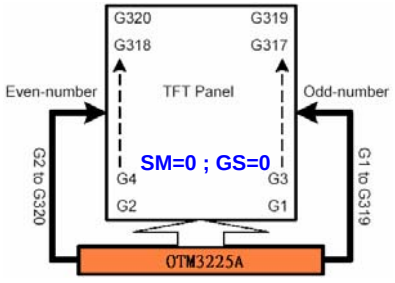
Table 6-2

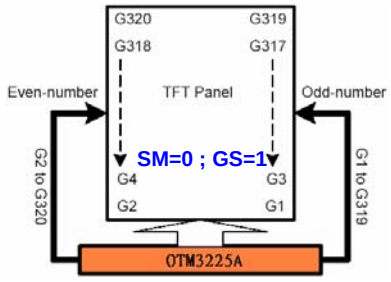
SS=0;BGR=0;	S1	S2	S3	···▶	S718	S719	S720
SS=0;BGR=1;	S1	S2	S3	···▶	S718	S719	S720
SS=1,BGR=0;	S1	S2	S3	◀···	S718	S719	S720
SS=1,BGR=1;	S1	S2	S3	◀···	S718	S719	S720

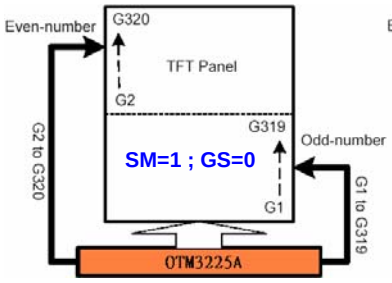
SM: Set the scan mode of the gate driver output. Moreover, SM can cooperate with GS for different LCD panel gate line layout. The combination of GS and SM bit are summarized at **Table 6-3 and Figure 6-6**.

Table 6-3

SM	GS	Gate output sequence (Begin,…..,End)
0	0	G1→G2→G3→G4→….→G317→G318→G319→G320
0	1	G320→G319→G318→G317→,…→G4→G3→G2→G1
1	0	G1→G3→G5→,…→G317→G319→ →G2→G4→G6→,...→G318→G320
1	1	G32()→G318→G316→….→G4→G2→ →G319→G317→G315→....→G3→G1







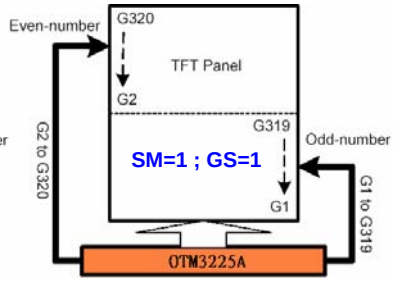


Figure 6-6 : Panel layout for SM & GS bit

6.2.4. LCD Driving Waveform Control (R02h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	1	BC0	EOR	0	0	0	0	0	0	0	0

BC0: This bit can set the VCOM toggle at ever frame format or N-line inversion format.

BC0=0: Frame inversion waveform is selected.

BC0=1: Line inversion waveform is selected. (Must combine EOR=1 for Line inversion)

EOR: Enables Line-inversion when EOR=1 and BC0=1.

6.2.5. Entry Mode (R03h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0

Table 6-4

Operation mode	ORG	AM	I/D1	I/D0	Function
Mode 1	0	0	0	0	Replace horizontal data
Mode2	0	1	0	1	Replace vertical data
Mode3	1	0	1	0	Conditionally replace horizontal data
Mode4	1	1	1	1	Conditionally replace vertical data

★**Note:** After changing ORG;AM;I/D1 or I/D0 bit, display data must be rewritten.

AM: To set the update direction when writing data to GRAM.

If AM=1, data will write in vertical direction. (Address counter will automatic update in vertical direction)

If AM=0, data will write in horizontal direction. (Address counter will automatic update in horizontal direction)

When setting a window area by register R50h~R53h, the data is written only within the area based on by I/D[1:0],AM bit.

I/D1-0: To specify address counter(AC) automatically increment or decrement while update one pixel display data to GRAM.

I/D[0] indicates the increment or decrement in horizontal direction.

I/D[0]=0: decrement in horizontal direction automatically

I/D[0]=1: increment in horizontal direction automatically

I/D[1] indicates the increment or decrement in vertical direction.

I/D[1]=0: decrement in vertical direction automatically

I/D[1]=1: increment in vertical direction automatically

ID[1-0] setting can cooperate with Am bit to set the data updating direction.

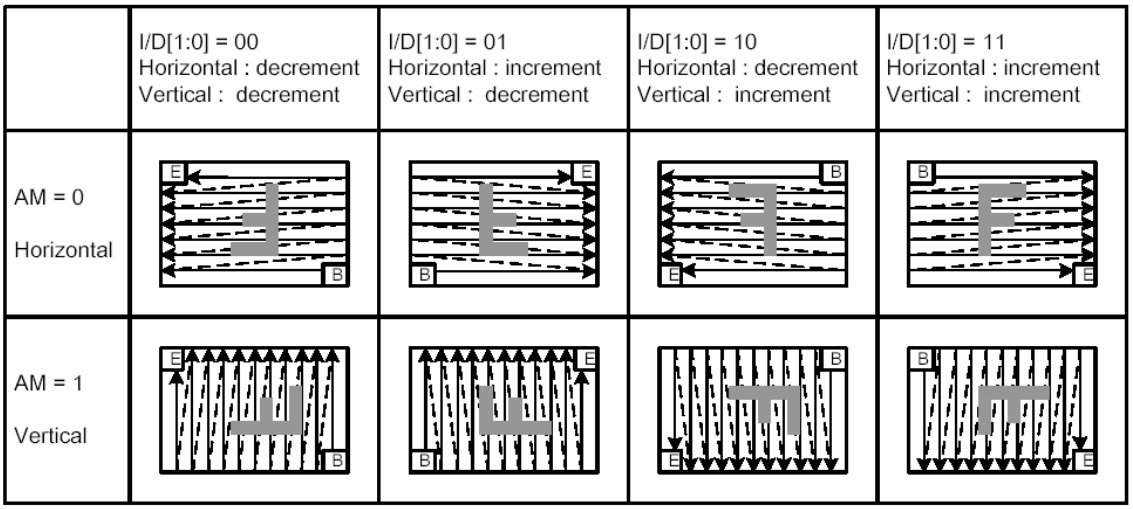


Figure 6.7

ORG: OTM3225A provides the option of start address definition when window function is selected.

ORG=0: RAM address setting (R20h, R21h) should set to the window start address, as normal operation case.

In this case, the origin address is not move.

ORG=1: RAM address setting (R20h, R21h) should set to (0x0000h) no matter where the window start address is.

Setting other addresses is inhibited.

In this case, the window start position is treated as (0x0000h), regardless the physical location in GRAM.

★**Note:** In GRAM read operation(R22h), make sure to set ORG=0.

★**Note:** In RGB mode with Full-Screen operation, make sure to set ORG=1.

BGR: To set the order of RGB sub-pixel in GRAM.

The combination of SS and BGR bit are summarized at **Table 6-2**.

BGR=0: same assignment of RGB allocation of DB17-0.

DB17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

BGR=1: inverse assignment of RGB allocation of DB17-0.

DB17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

Figure 6.8

DFM: In combination with TRI setting, sets the format to develop 16-/8-bit data to 18-bit data when using either 16-bit or 8-bit bus interface. Make sure to set DFM=0 when not transferring data via 16-bit or 8-bit interface.

TRI: to set 1–3 time transfer mode for system interface. TRI bit should cooperate with DFM to meet the specific transfer mode.

For 8-bit data bus interface mode:

TRI=0: 2 time transfer mode for 16-bit GRAM data.

TRI=1: 3 time transfer mode for 18-bit GRAM data

For 16-bit data bus interface mode:

TRI=0: 1 time transfer mode for 16-bit GRAM data.

TRI=1: 2 time transfer mode for 18-bit GRAM data

★**Note:** Set TRI=0, when using neither 8-bit nor 16-bit.

★**Note:** The combination of DFM and TRI bit are summarized at **Table 6-2**.

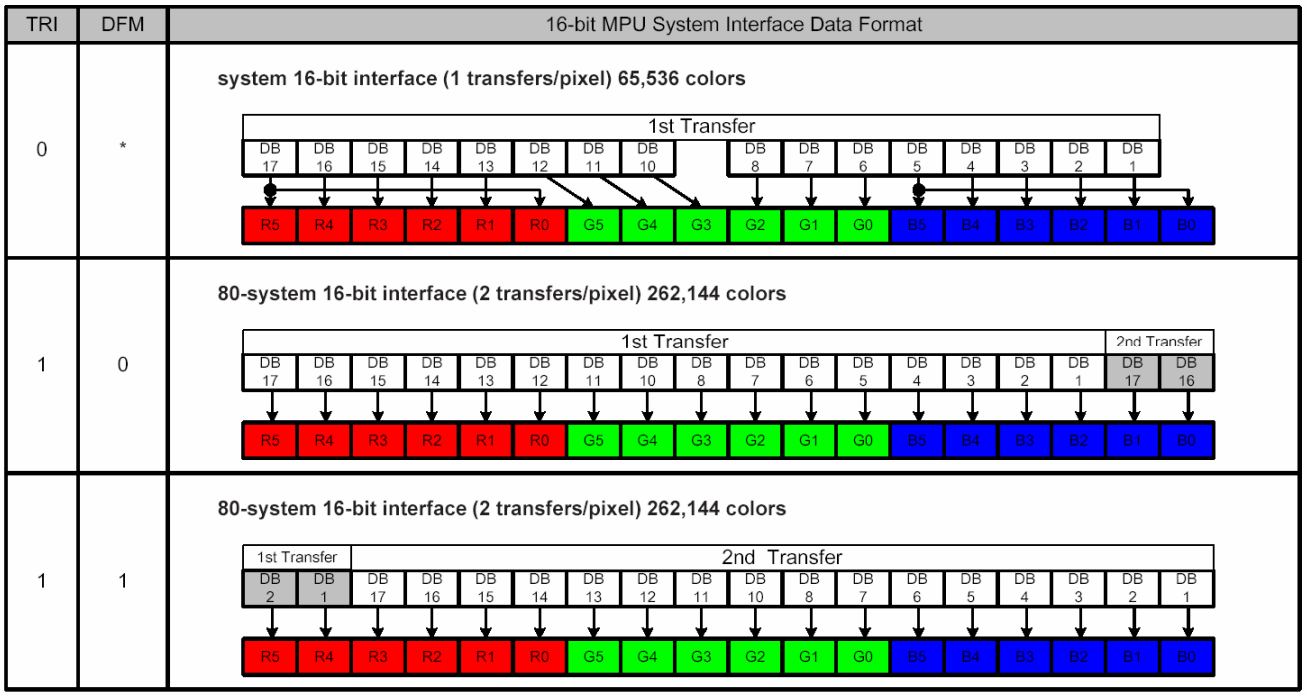


Figure 6.9

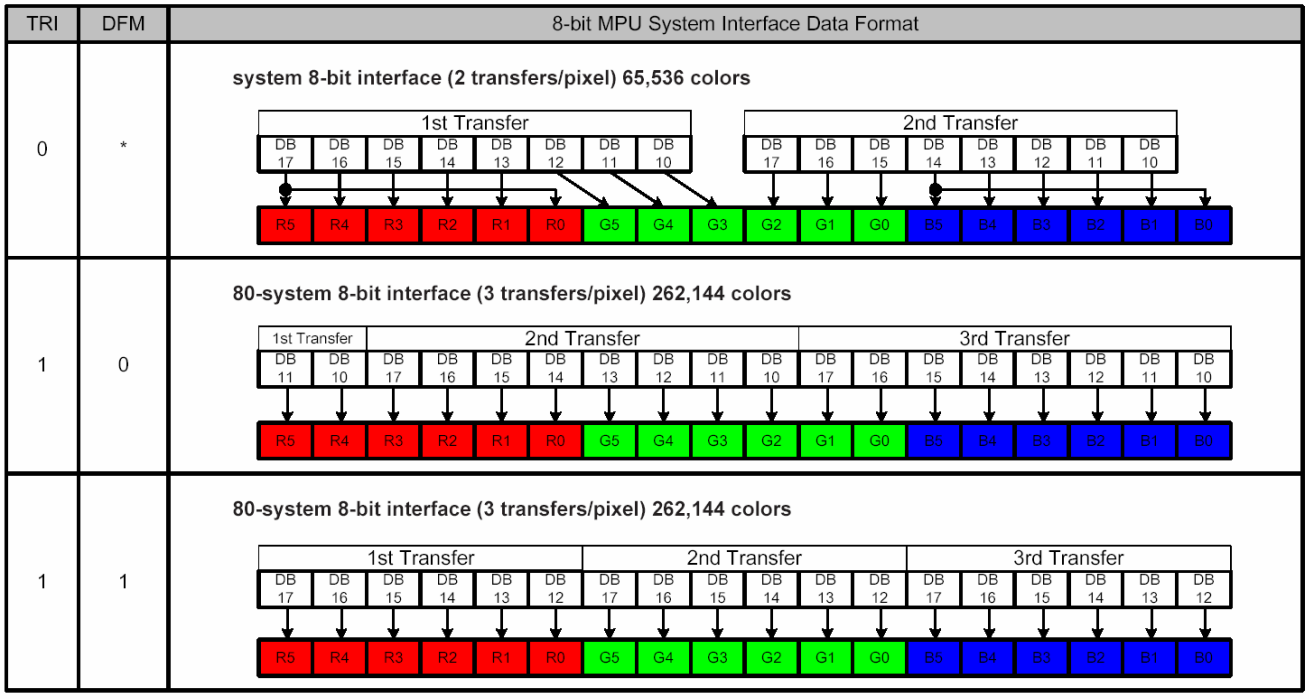


Figure 6.10

6.2.6. Scaling Control register (R04h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0

RSZ [1:0]: OTM3225A provides scaling factor to give the display more flexibility to show different picture size. For detail, refer to “Scaling function”.

RSZ1	RSZ0	Scaling Factor
0	0	No Scaling
0	1	1/2 times
1	0	Setting Disable
1	1	1/4 times

RCH [1:0]: To set the surplus pixel number in horizontal direction when scaling mode is selected. When scaling mode is not selected, make sure RCH [1:0]= “00”

RCH1	RCH0	Surplus pixel number in Horizontal direction
0	0	0 Pixel
0	1	1 Pixel
1	0	2 Pixels
1	1	3 Pixels

RCV [1:0]: To set the surplus pixel number in Vertical direction when scaling mode is selected. When scaling mode is not selected, make sure RCV [1:0]= “00”

RCV1	RCV0	Surplus pixel number in Vertical direction
0	0	0 Pixel
0	1	1 Pixel
1	0	2 Pixels
1	1	3 Pixels

6.2.7. Display Control (R07h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	COL	0	D1	D0

D1-0: To set the internal operation, source driver output and VCOM output function. When D1-0=00; OTM3225A is set to standby mode. The combination of D1 and AM bit is summarized at **Table 6-5**.

Table 6-5

D1	BASEE	Source, VCOM output	Internal Operation	FLM
0	*	GND	Terminated	OFF
1	0	Non-lit display	Normal Operation	ON
	1	Normal display	Normal Operation	ON

COL: 8-color mode selection. When CL=1 OTM3225A enter to 8-color mode. When CL=0, OTM3225A is in normal operation mode.

DTE: Specify the high/low level of gate driver output signal. The meaning of DTE bit is summarized at **Table 6-6**

Table 6-6

APE	DTE	Gate Output
1	0	VGL
	1	VGH/VGL

BASEE: To enable Base image display

BASEE	Display
0	(1) Non-lit display (2) Partial image display
1	Base image is display on the LCD

PTDE1-0: To set the partial-display enables function.

PTDE [0]: "0" Partial image 1 display "Off".
"1" Partial image 1 display "On".

PTDE [1]: "0" Partial image 2 display "Off".
"1" Partial image 2 display "On".

6.2.8. Display Control 2 (R08h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

FP3-0: Set the amount of blank period of front porch

BP3-0: Set the amount of blank period of back porch

Table 6-7 summarized the function of FP3-0/BP3-0 setting.

When setting this register, make sure that:

BP + FP ≤ 16 lines

FP ≥ 2 lines

BP ≥ 2 lines

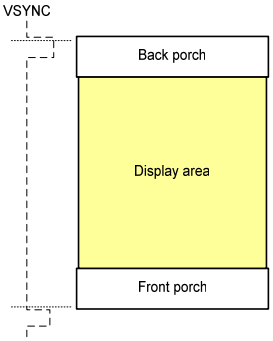


Figure 6-11 Front porch and back porch function diagram

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal. Be aware that different interface mode, has different BP/ FP setting. **Table 6-8** summarized the setting for each interface mode.

Table 6-7

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	**BP2**	**BP1**	**BP0**	**Number of lines for the Back Porch**
0	0	0	0	1 lines
0	0	0	1	1 lines
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
0	1	0	1	5 lines
0	1	1	0	6 lines
0	1	1	1	7 lines
1	0	0	0	8 lines
1	0	0	1	9 lines
1	0	1	0	10 lines
1	0	1	1	11 lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	15 lines

Table 6-8

Operation of Internal clock	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
RGB interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
VSYNC interface	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP = 16 lines

6.2.9. Display Control 3 (R09h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

ISC3-0: To set the gate driver scan cycle in non-display area.

Table 6-9 summarized the function of ISC3-0 setting

Table 6-9

ISC3	ISC2	ISC1	ISC0	Scan cycle	fFLM=60Hz
0	0	0	0	1 Frames	16ms
0	0	0	1	1 Frames	16ms
0	0	1	0	3 Frames	50 ms
0	0	1	1	5 Frames	84 ms
0	1	0	0	7 Frames	117 ms
0	1	0	1	9 Frames	150 ms
0	1	1	0	11 Frames	184 ms
0	1	1	1	13 Frames	217 ms
1	0	0	0	15 Frames	251 ms
1	0	0	1	19 Frames	317 ms
1	0	1	0	21 Frames	351 ms
1	0	1	1	23 Frames	384 ms
1	1	0	0	25 Frames	418 ms
1	1	0	1	27 Frames	451 ms
1	1	1	0	29 Frames	484 ms
1	1	1	1	31 Frames	518 ms

PTG1-0: To set the gate driver scan mode in non-display area.

Table 6-10 summarized the function of PTG1-0 setting

Table 6-10

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
0	1	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
1	0	Interval scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
1	1	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML

PTS2-0: To set the source driver output level in non-display area of partial display mode. **Table 6-11** summarized the function of PTS2-0 setting.

Table 6-11

PTS2	PTS1	PTS0	Source output in non-display area		Operation amplifier in non-display area	Display in non-display area (Normally White panel)
			+ polarity	- polarity		
0	0	0	V63	V0	V0~V63	White
0	0	1	V0	V63	V0~V63	Black
0	1	0	GND	GND	V0~V63	White
0	1	1	High impedance	High impedance	V0~V63	Abnormal (Crosstalk)
1	0	0	V63	V0	V0~V63	White
1	0	1	V0	V63	V0~V63	Black
1	1	0	GND	GND	V0~V63	White
1	1	1	High impedance	High impedance	V0~V63	Abnormal (Crosstalk)

6.2.10. Frame Cycle Control (R0Ah)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0

FMI [2:0]: (FMark Interval) OTM3225A provide FMARK signal to prevent tearing effect. FMI [2:0] can set FMARK output interval.

FMI2	FMI1	FMI0	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	0	3 frames
0	1	1	4 frames
1	0	0	5 frames
1	0	1	6 frames
1	1	0	7 frames
1	1	1	8 frames

FMARKOE: (FMARK Output Enable) Set the output signal FMARK from FMARK pin.

FMARK="0": Stop to output FMARK signal.

FMARK="1". Start to output FMARK signal.

6.2.11. External Display Interface Control 1 (R0Ch)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

RIM1-0: To set the different transfer modes of RGB interface. **Table 6-**12 summarized the function of RIM1-0 setting.

Table 6-12

RIM1	RIM0	RGB Interface Mode	Colors	Data Bus	Number of transfer during 1 line
0	0	18-bit RGB interface (one transfer/pixel)	262K	DB 17-0	240x18-bits (AM bit=0) 320x18-bits (AM bit=1)
0	1	16-bit RGB interface (one transfer/pixel)	65K	DB 17-13; DB 11-1	240x16-bits (AM bit=0) 320x16-bits (AM bit=1)
1	0	6-bit RGB interface (three transfers/pixel)	262K	DB17-12	720x6-bits (AM bit=0) 960x6-bits (AM bit=1)
1	1	8-bit RGB interface (two transfers/pixel)	65K	DB17-10	480x8-bits (AM bit=0) 640x8-bits (AM bit=1)

DM1-0: To specify the display interface mode. DM1-0 Setting can switch the display interface among system interface, RGB interface and VSYNC interface. **Table 6-13** summarized the function of DM1-0 setting.

Table 6-13

DM1	DM0	Display Interface
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RM: Select the interface to access the OTM3225A's internal GRAM. Set RM to "1" when writing display data via the RGB interface. The OTM3225A allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possible to rewrite display data via a system interface by setting RM = "0" even while display operations are performed via the RGB interface.
Table 6-14 summarized the function of RM bit setting.

Table 6-14

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

Table 6-15

Display State	Operation Mode	RAM access Mode(RM)	Display operation Mode (DM1-0)
Still pictures	Internal clock	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving pictures	RGB interface	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)
Low Speed moving picture	RGB interface	RGB interface (RM = 1)	Internal clock operation (DM1-0 = 00)

Note1: Instructions are set only via the system interface.
Note2: Do not make changes to the RGB-I/F mode setting (RIM-0) while the RGB I/F is in operation.
Note3: See the "External Display Interface" section for the flowcharts to follow when switching from one mode to another.

6.2.12. Frame Maker Position (R0Dh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0

FMP 8-0: Indicates the output position of frame cycle signal (FMARK).

A high-active pulse is output from FMARK pin and It's relate with back porch.

When FMP[8:0] =9'h000, FMARK is outputted at the start of back porch for 1line period.

When FMP[8:0] =9'h001, FMARK is outputted one line after the start of back porch.

Please reference "9.1. FMARK function" for detail description.

FMP [8:0]	FMARK Output Position
9'h000	Immediate (Delay 0 line period)
9'h001	Delay 1 line period
9'h002	Delay 2 lines period
	~
Max. Vaule	9'h000≦FMP[8:0]≦BP+NL+FP

6.2.13. External Display Interface Control 2 (R0Fh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

EPL: The polarity of ENABLE signal selection in RGB interface mode.

EPL = "0": ENABLE: Low active

EPL = "1": ENABLE: High active

DPL: Select the data latch edge of the DOTCLK signal in RGB interface mode.

DPL = "0": rising edge of the DOTCLK.

DPL ="1": falling edge of the DOTCLK.

VSPL: The polarity of VSYNC signal selection in RGB interface mode.

VSPL = "0": Low active.

VSPL = "1": High active.

HSPL: The polarity of HSYNC signal selection in RGB interface mode.

HSPL = "0": Low active.

HSPL = "1": High active.

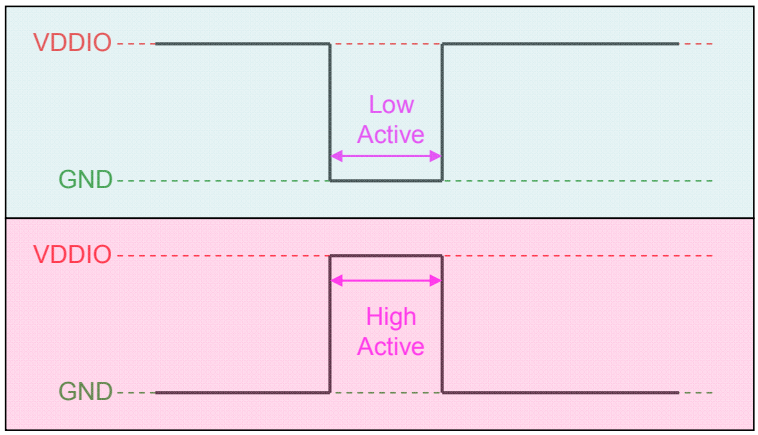


Figure 6.12

6.2.14. Power Control 1 (R10h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB

SLP: Sleep mode selection. When SLP =1, OTM3225A set to sleep mode. In sleep mode, all internal operations are terminated except internal RC oscillation. Be sure that a display off sequence should be executed before set SLP to “1”. In sleep mode, no instruction can be accepted except R11h, R13h, bit 3-0 of R12h and R10h (except SAP2-0). Set STB=0 can exit sleep mode. Moreover, when exit from sleep mode, data in GRAM and in instruction registers are keep the same with these before set to SLP mode.

STB: Standby mode selection. When STB =1, OTM3225A set to standby mode. In this mode, all internal operations are terminated including internal RC oscillation. Be sure that a display off sequence should be executed before set STB to “1”. Set STB=0 can exit standby mode. Be sure that start oscillation following by 10ms delay should be executed before set STB to “0”. Moreover, when exit from standby mode, data in GRAM and register will not lost, reset and re-sending command and data into GRAM is not necessary.

AP2-0: Operational amplifier DC bias current adjustment. Set AP2-0 = “000” to stop operational amplifier and DC/DC charge pump circuits to reduce current consumption during no display period.

APE: Enable bit for both liquid crystal power supply and gamma voltage generation circuit.

APE=”0”, Halt liquid crystal power supply and gamma voltage generation circuit

APE=”1”, Enable liquid crystal power supply and gamma voltage generation circuit.

BT3-0: Set the voltage level of DDVDH, VGH, VGL and VCL.

Table 6-16 summarized the function of BT3-0 setting

BT2	BT1	BT0	DDVDH	VGH	VGL	VCL
0	0	0	VCI1 x 2	VCI1 x 6	VCI1x -5	-VCI1
0	0	1	VCI1 x 2	VCI1 x 6	VCI1x -4	-VCI1
0	1	0	VCI1 x 2	VCI1 x 6	VCI1x -3	-VCI1
0	1	1	VCI1 x 2	VCI1 x 5	VCI1x -5	-VCI1
1	0	0	VCI1 x 2	VCI1 x 5	VCI1x -4	-VCI1
1	0	1	VCI1 x 2	VCI1 x 5	VCI1x -3	-VCI1
1	1	0	VCI1 x 2	VCI1 x 4	VCI1x -4	-VCI1
1	1	1	VCI1 x 2	VCI1 x 4	VCI1x -3	-VCI1

SAP: Enable bit for gamma voltage generation circuit.

SAP=”0”, Halt gamma voltage generation circuit.

SAP=”1”, Enable gamma voltage generation circuit

6.2.15. Power Control 2 (R11h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0

VC2-0: Set the voltage of VCIOUT. VCIOUT is generated by VCI. **Table 6-17** summarized the function of VC2-0 setting

Table 6-17

VC2	VC1	VC0	VCIOUT
0	0	0	0.95 x VCI
0	0	1	0.9 x VCI
0	1	0	0.85 x VCI
0	1	1	0.8 x VCI
1	0	0	0.75 x VCI
1	0	1	0.7 x VCI
1	1	0	0.65 x VCI
1	1	1	1.00 x VCI

DC02-00: Set DC/DC charge pump circuit 1 operating frequency. **Table 6-18** summarized the function of DC02-00 setting

Table 6-18

DC02	DC01	DC00	DC/DC charge pump circuit 1 frequency (fDCDC1)
0	0	0	2H
0	0	1	1H
0	1	0	1/2H
0	1	1	1/4H
1	0	0	1/8H
1	0	1	1/16H
1	1	0	1/32H
1	1	1	1/64H

DC12-10: Set DC/DC charge pump circuit 2 operating frequency. **Table 6-19 s**ummarized the function of DC02-00 setting
Note: Be aware that DC/DC charge pump 1 frequency ≥ DC/DC charge pump 2 frequency

Table 6-19

DC12	DC11	DC10	Step-up circuit 2 step-up frequency (fDCDC2)
0	0	0	1H
0	0	1	1/2H
0	1	0	1/4H
0	1	1	1/8H
1	0	0	1/16H
1	0	1	1/32H
1	1	0	1/64H
1	1	1	1/128H

Note: Be sure fDCDC1≥fDCDC2 when setting DC02-00, DC12-10.
CPU mode : 1H= Fosc / RTNI*DIVI
RGB mode : 1H= Fosc / RTNE*DIVE

6.2.16. Power Control 3 (R12h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	1	VRH3	VRH2	VRH1	VRH0

VCIRE: Select reference voltage for VREG1OUT

VCIRE = “0” (default): External VCI as reference voltage for VREG1OUT.

VCIRE = ”1”: Internal VCIR as reference voltage for VREG1OUT. (VCIR=2.5V)

VRH3-0: Set the voltage level of VCI. VCI is generated by VREG1OUT. **Table 6-20** summarized the function of VRH3-0 setting

Table 6-20

VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage	
				VCIRE=0	VCIRE=1
0	0	0	0	Halt	Halt
0	0	0	1	VCIx2.00	2.5Vx2.00 = 5.000V
0	0	1	0	VCIx2.05	2.5Vx2.05 = 5.125V
0	0	1	1	VCIx2.10	2.5Vx2.10 = 5.250V
0	1	0	0	VCIx2.20	2.5Vx2.20 = 5.500V
0	1	0	1	VCIx2.30	2.5Vx2.30 = 5.750V
0	1	1	0	VCIx2.40	2.5Vx2.40 = 6.000V
0	1	1	1	VCIx2.40	2.5Vx2.40 = 6.000V
1	0	0	0	VCIx1.60	2.5Vx1.60 = 4.000V
1	0	0	1	VCIx1.65	2.5Vx1.65 = 4.125V
1	0	1	0	VCIx1.70	2.5Vx1.70 = 4.250V
1	0	1	1	VCIx1.75	2.5Vx1.75 = 4.375V
1	1	0	0	VCIx1.80	2.5Vx1.80 = 4.500V
1	1	0	1	VCIx1.85	2.5Vx1.85 = 4.625V
1	1	1	0	VCIx1.90	2.5Vx1.90 = 4.750V
1	1	1	1	VCIx1.95	2.5Vx1.95 = 4.875V

6.2.17. Power Control 4 (R13h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0

VDV4-0: Set the Vcom amplitude. Vcom amplitude is generated by VREG1OUT.

Table 6-21

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VREG1OUT x 0.70
0	0	0	0	1	VREG1OUT x 0.72
0	0	0	1	0	VREG1OUT x 0.74
0	0	0	1	1	VREG1OUT x 0.76
0	0	1	0	0	VREG1OUT x 0.78
0	0	1	0	1	VREG1OUT x 0.80
0	0	1	1	0	VREG1OUT x 0.82
0	0	1	1	1	VREG1OUT x 0.84
0	1	0	0	0	VREG1OUT x 0.86
0	1	0	0	1	VREG1OUT x 0.88
0	1	0	1	0	VREG1OUT x 0.90
0	1	0	1	1	VREG1OUT x 0.92
0	1	1	0	0	VREG1OUT x 0.94
0	1	1	0	1	VREG1OUT x 0.96
0	1	1	1	0	VREG1OUT x 0.98
0	1	1	1	1	VREG1OUT x 1.00
1	0	0	0	0	VREG1OUT x 0.94
1	0	0	0	1	VREG1OUT x 0.96
1	0	0	1	0	VREG1OUT x 0.98
1	0	0	1	1	VREG1OUT x 1.00
1	0	1	0	0	VREG1OUT x 1.02
1	0	1	0	1	VREG1OUT x 1.04
1	0	1	1	0	VREG1OUT x 1.06
1	0	1	1	1	VREG1OUT x 1.08
1	1	0	0	0	VREG1OUT x 1.10
1	1	0	0	1	VREG1OUT x 1.12
1	1	0	1	0	VREG1OUT x 1.14
1	1	0	1	1	VREG1OUT x 1.16
1	1	1	0	0	VREG1OUT x 1.18
1	1	1	0	1	VREG1OUT x 1.20
1	1	1	1	0	VREG1OUT x 1.22
1	1	1	1	1	VREG1OUT x 1.24

6.2.18. GRAM Address Set (Horizontal Address) (R20h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

6.2.19. GRAM Address Set (Vertical Address) (R21h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD16–0: To set the initial address counter for GRAM address. Based on AM and I/D[1:0] setting, the address counter is automatically increment or decrement while data are written to the internal GRAM. There is no need to updated AD16-0 every data transfer if AD16-0 was set in the beginning of one frame graphic data. Be aware that address counter is not automatically updated if reading data from the internal GRAM instruction is executed. Moreover, the address counter cannot be accessed when the OTM3225A is in standby mode.

Table 6-22 summarized the function of AD15-0 setting

Table 6-22

AD[16:0]	GRAM data map
17'h00000 – 17'h000EF	1st line GRAM data
17'h00100 –17'h001EF	2nd line GRAM data
17'h00200 –17'h002EF	3rd line GRAM data
17'h00300 –17'h003EF	4th line GRAM data
:	:
17'h13600 –17'h13CEF	317th line GRAM data
17'h13700 –17'h13DEF	318th line GRAM data
17'h13800 –17'h13EEF	319th line GRAM data
17'h13900 –17'h13FEF	320th line GRAM data

6.2.20. Write Data to GRAM (R22h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM write data (WD17-0) The DB17-0 pin assignment is different in different interface modes.															

WD17-0: OTM3225A supports 18 bits data format. However, if only 16-bit (565format) is input to GRAM, OTM3225A will expand the 16 bit data into 18-bit format. Same case when RGB interface is selected. Based on the graphic data in GRAM, the grayscale voltage of source driver is selected. **Table 6-23** summarized the source driver grayscale voltage output versus graphic data in GRAM. **Figure 613 ~ Figure 626** illustrates the pin assignment among data bus (DB17-0), R22 (WD17-0) and GRAM.

Table 6-23

Data in GRAM	Source Driver Grayscale Output	
RGB	Negative	Positive
000000	V0	V63
000001	V1	V62
000010	V2	V61
000011	V3	V60
000100	V4	V59
000101	V5	V58
000110	V6	V57
000111	V7	V56
001000	V8	V55
001001	V9	V54
001010	V10	V53
001011	V11	V52
001100	V12	V51
001101	V13	V50
001110	V14	V49
001111	V15	V48
010000	V16	V47
010001	V17	V46
010010	V18	V45
010011	V19	V44
010100	V20	V43
010101	V21	V42
010110	V22	V41
010111	V23	V40
011000	V24	V39
011001	V25	V38
011010	V26	V37
011011	V27	V36
011100	V28	V35
011101	V29	V34
011110	V30	V33
011111	V31	V32
100000	V32	V31
100001	V33	V30
100010	V34	V29
100011	V35	V28
100100	V36	V27
100101	V37	V26
100110	V38	V25
100111	V39	V24
101000	V40	V23
101001	V41	V22
101010	V42	V21
101011	V43	V20
101100	V44	V19
101101	V45	V18
101110	V46	V17
101111	V47	V16
110000	V48	V15
110001	V49	V14
110010	V50	V13
110011	V51	V12
110100	V52	V11
110101	V53	V10
110110	V54	V9
110111	V55	V8
111000	V56	V7
111001	V57	V6
111010	V58	V5
111011	V59	V4
111100	V60	V3
111101	V61	V2
111110	V62	V1
111111	V63	V0

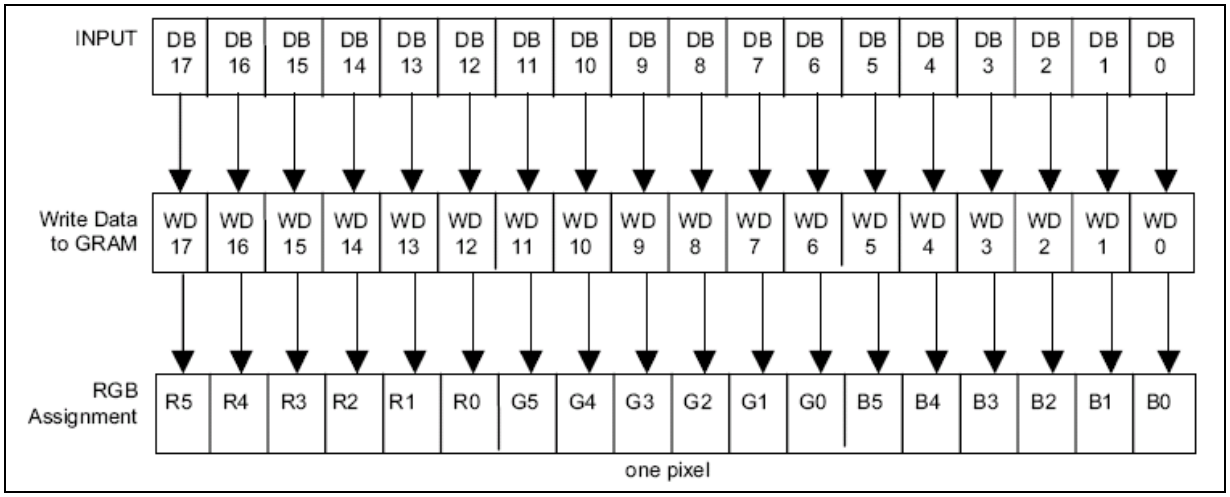


Figure 6.13 18-bit interface (262,144 colors) TRI = 0, DFM=x.

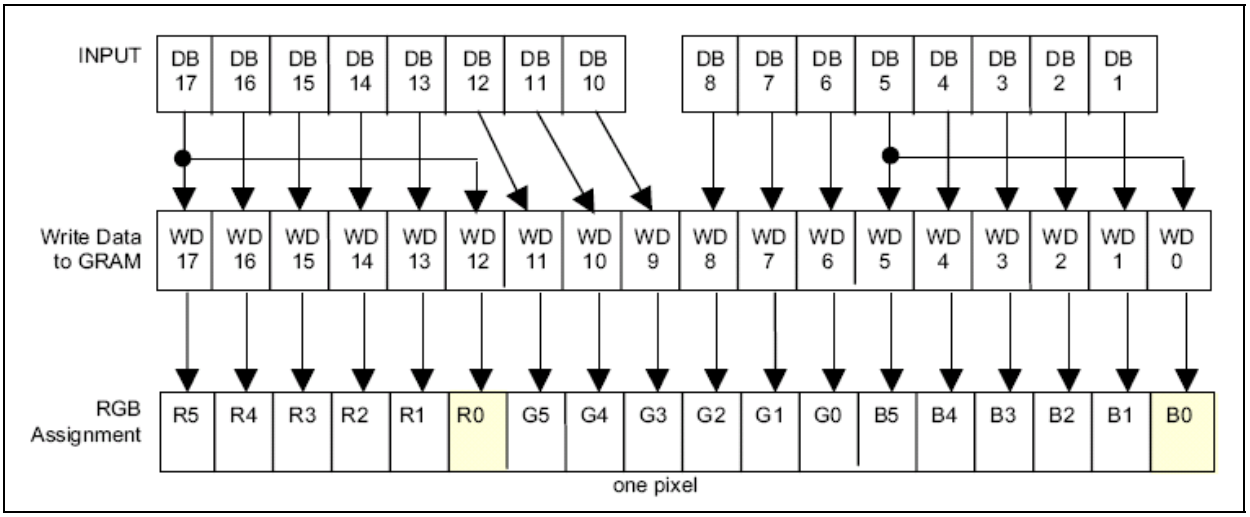


Figure 6.14 16-bit interface (65,536 colors) TRI= 0 , DFM=x

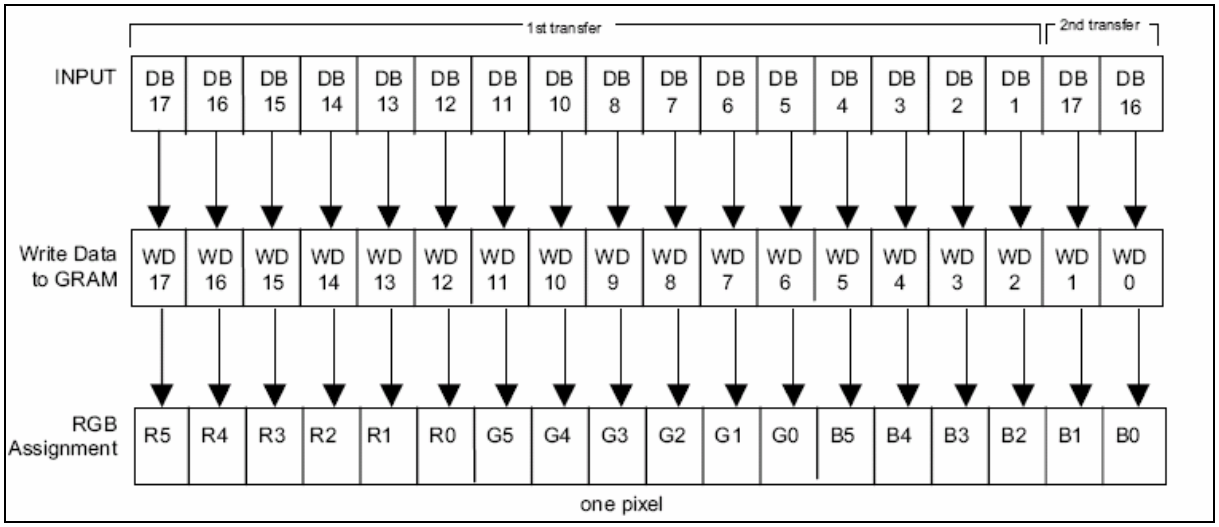


Figure 6.15 16-bit interface (262,144 colors) TRI = 1, DFM = 0

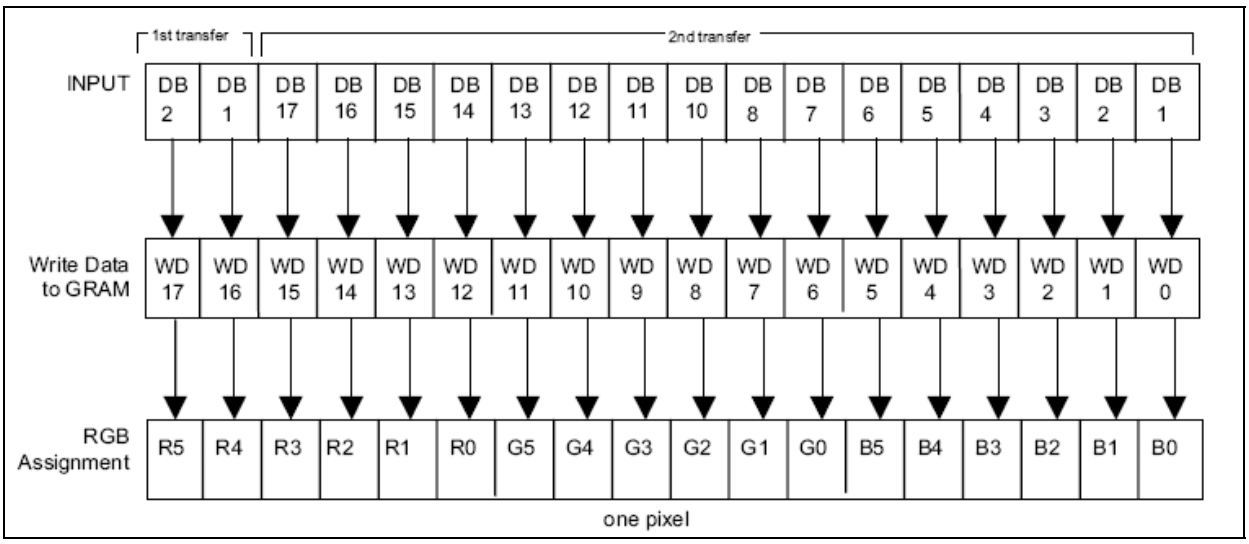


Figure 6.16 16-bit interface (262,144 colors) TRI = 1, DFM = 1

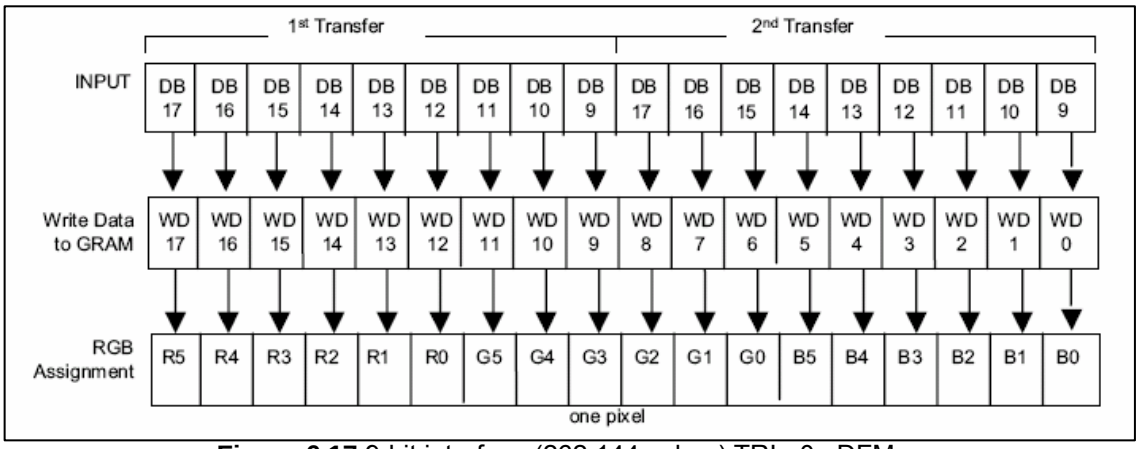


Figure 6.17 9-bit interface (262,144 colors) TRI= 0 , DFM=x

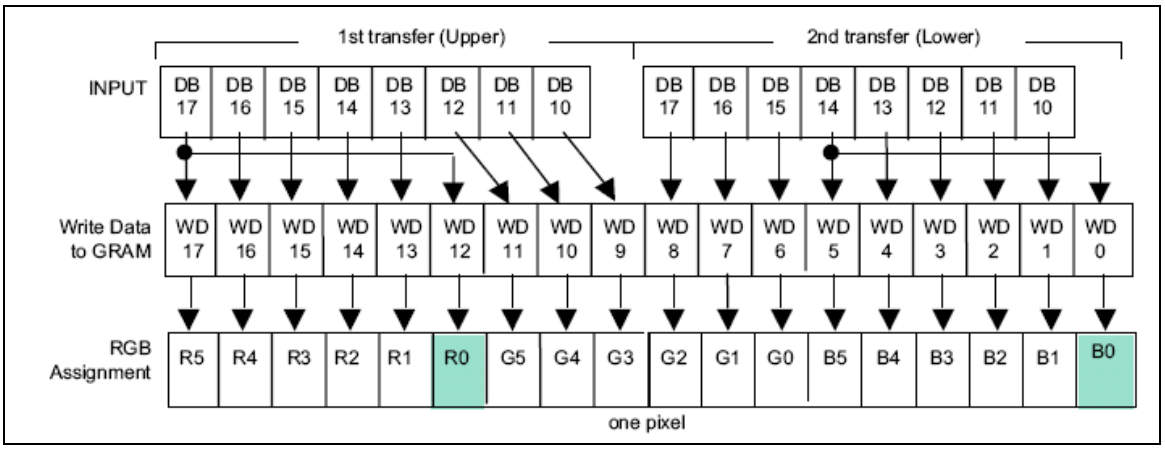


Figure 6.18 8-bit interface (65,536 colors) TRI = 0, DFM=x

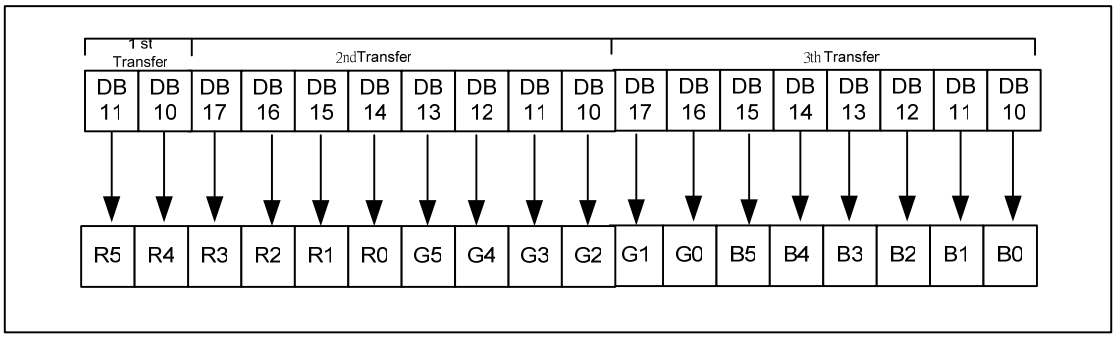


Figure 6.19 8-bit interface (262,144 colors) TRI = 1, DFM=0.

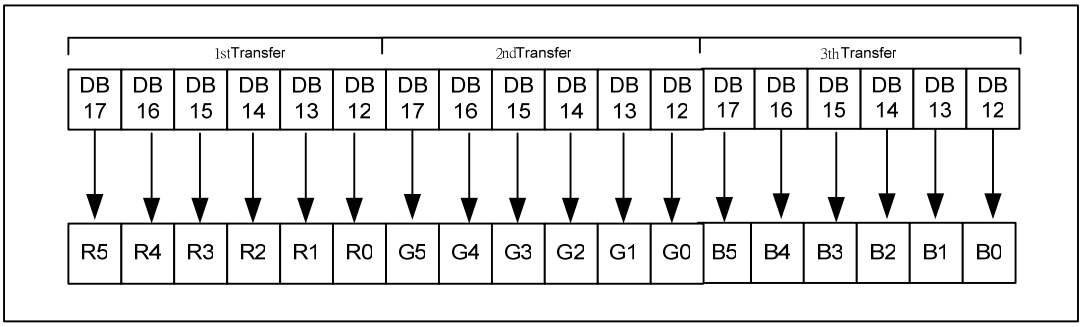


Figure 6.20 8-bit interface (262,144 colors) TRI = 1, DFM=1

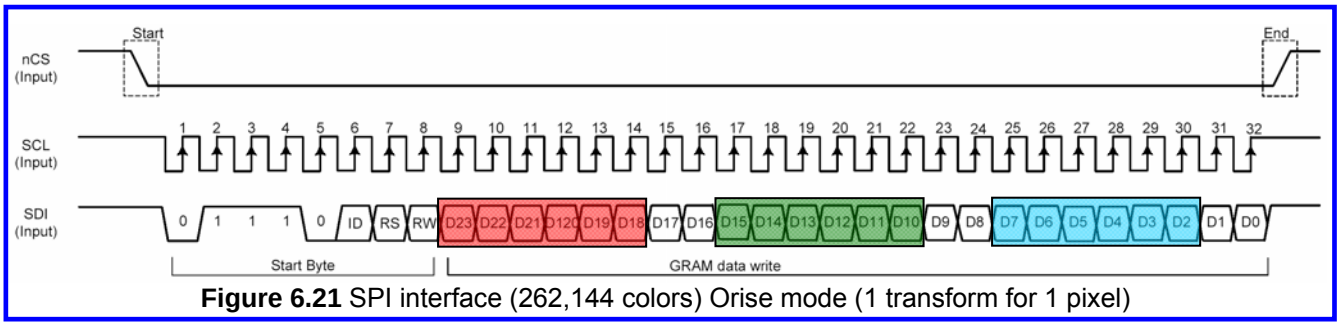


Figure 6.21 SPI interface (262,144 colors) Orise mode (1 transform for 1 pixel)

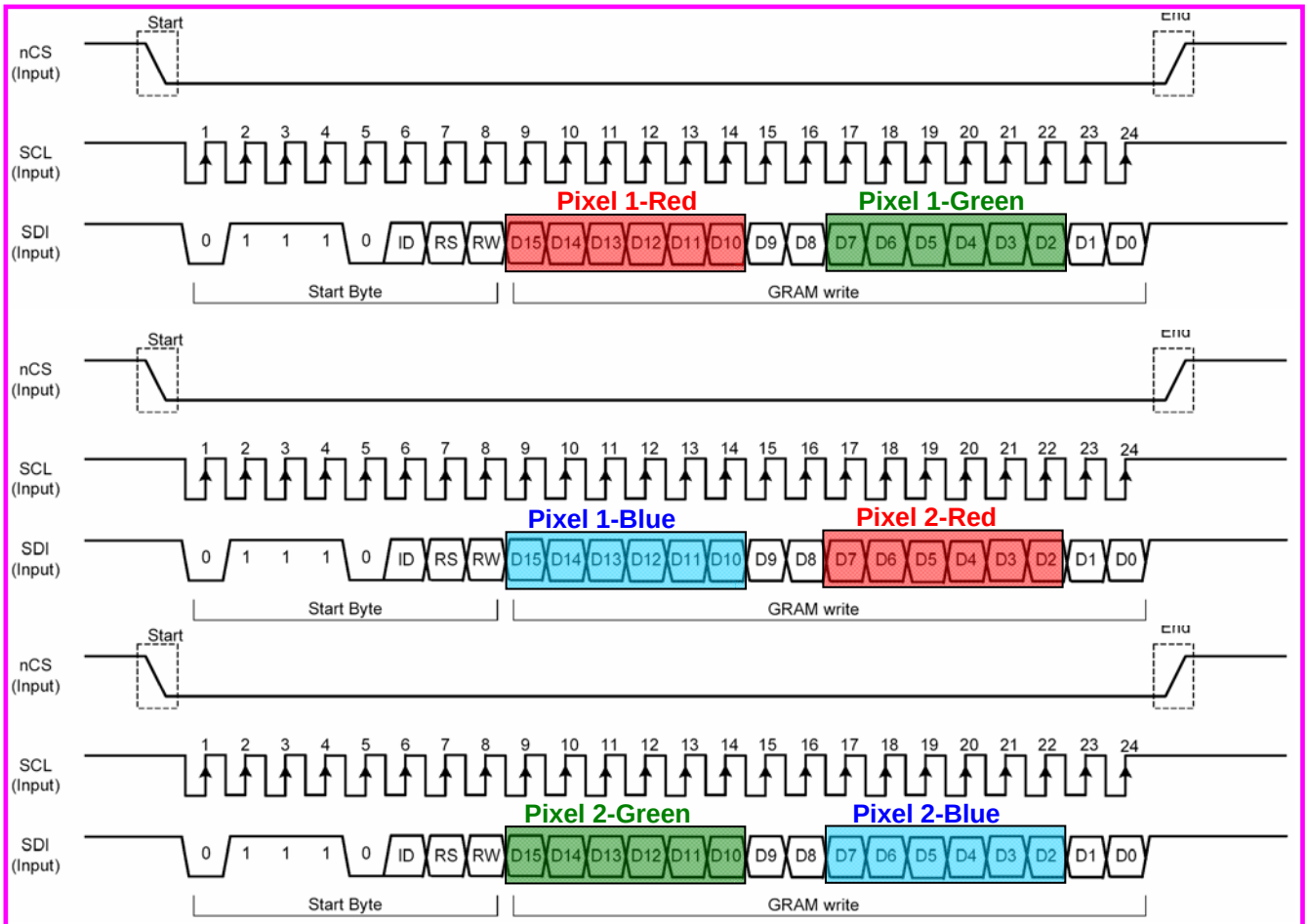


Figure 6.22 SPI interface (262,144 colors) Orise mode (3 transform for 2 pixels)

★**Orise Mode:** Please contact OriseTech and request the initial code for the SPI 262K mode.

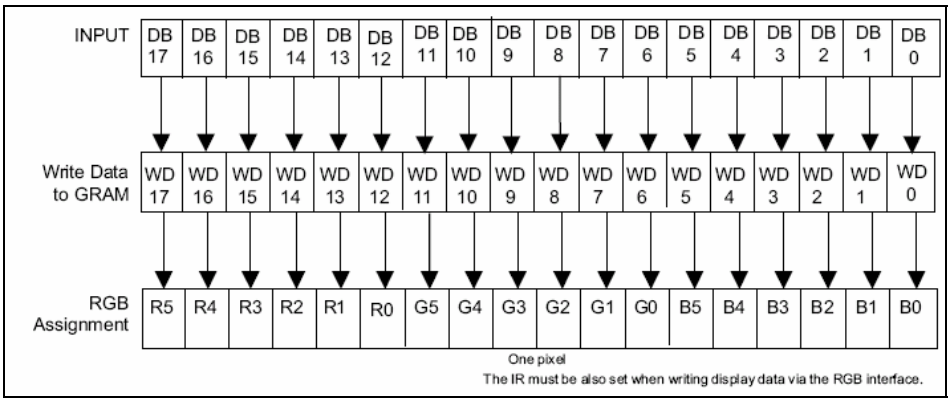


Figure 6.23 18-bit RGB interface (262,144 colors) ; RIM=00

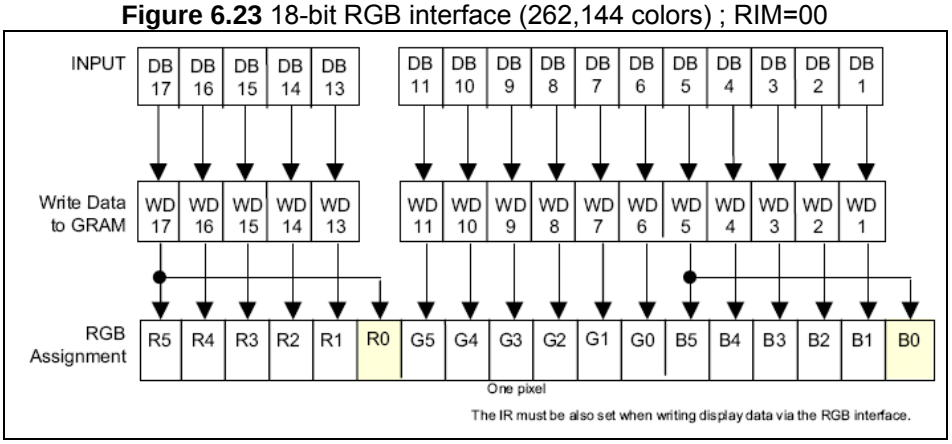


Figure 6.24 16-bit RGB interface (65,563 colors) ; RIM=01

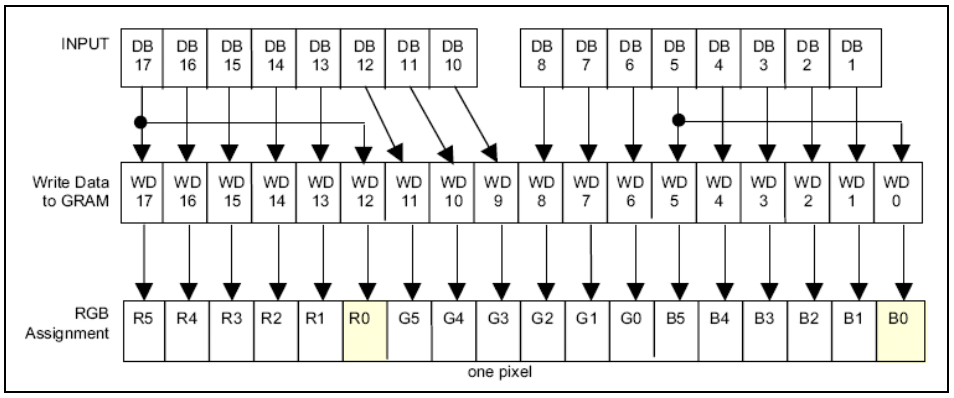


Figure 6.25 8-bit RGB interface (65,563 colors) ; RIM=11

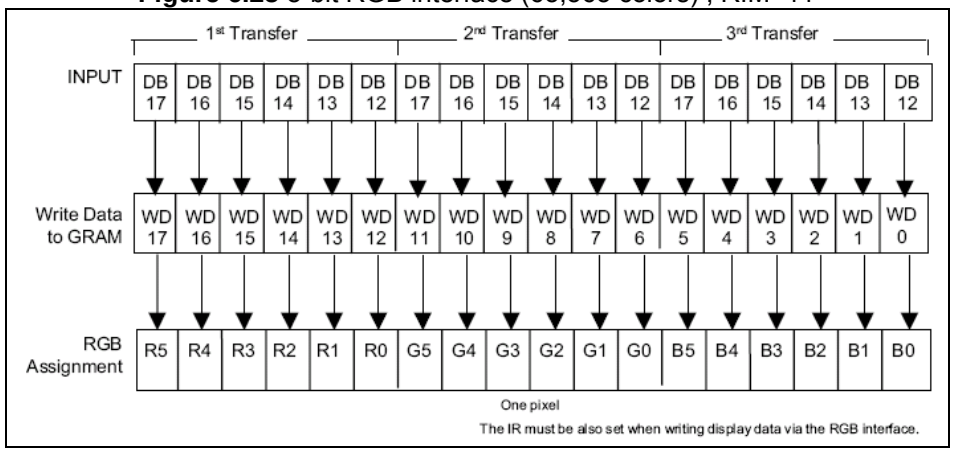


Figure 6.26 6-bit RGB interface (262,144 colors) ; RIM=10

OTM3225A supports external (RGB) interface. In RGB interface mode, all graphic data are stored in GRAM. To meet the diverse requirement of small size LCD panel, OTM3225A also supports in a fix window using RGB interface and outside the window still use system interface.

In RGB interface mode, data writing to the internal RAM is synchronized with DOTCLK during ENABLE = “Low”. Set ENABLE “High” to terminate writing data to RAM. Wait for a write/read bus cycle time. If accessing internal RAM using the RGB interface is desired after accessing the RAM via the system interface. **Figure 6.27** illustrates the timing diagram while RGB and system interface are both use in the same time.

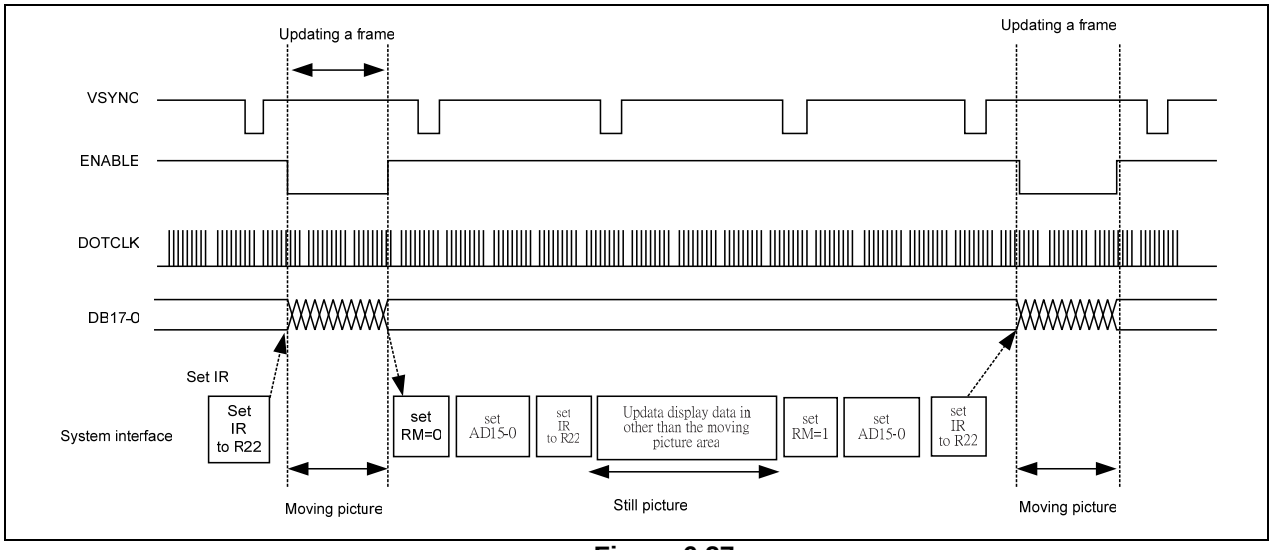


Figure 6.27

6.2.21. Read Data Read from GRAM (R22h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	1	RAM Read data (RD17-0) The DB17-0 pin assignment is different in different interface modes.															

R22 also served as a register, which store the data read out from GRAM. When data are read out from the GRAM is desired, first sets the RAM address and executes first word read, and issues second word read. When first word read instruction is issued, Invalid data are sent to the data bus DB17-0. Valid data are sent to the data bus as second word data is executed.

Note 1: The LSBs of R and B dots cannot read out, when the 8 or 16-bit interface is selected,

Note 2: This register is not available with the RGB interface. **Figure 6.28 ~ Figure 6.31** illustrates the pin assignment among data bus (DB17-0), R22 (RD17-0) and GRAM in read data instruction.

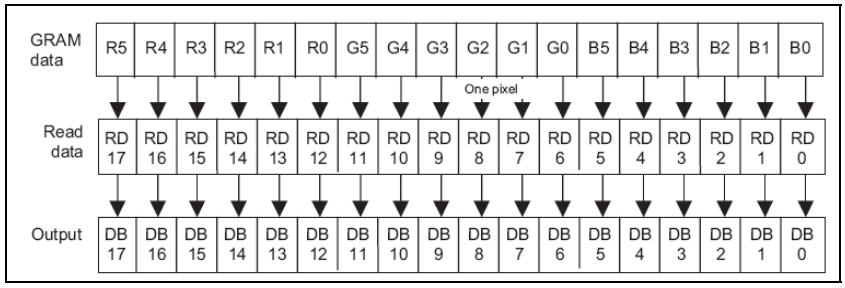


Figure 6.28 18-bit interface

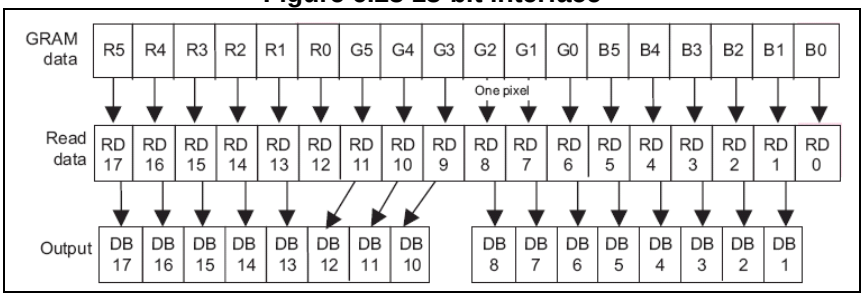


Figure 6.29 16-bit interface

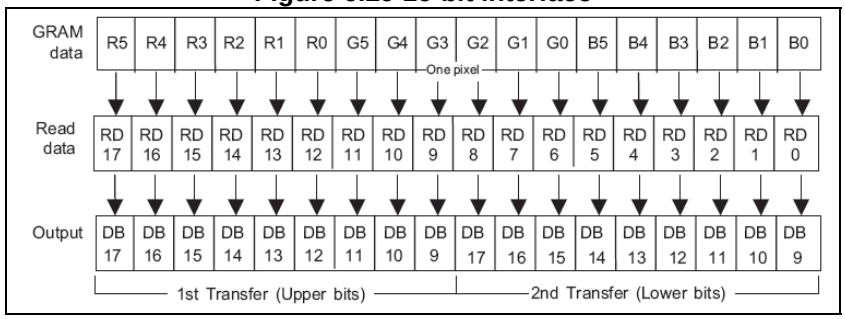


Figure 6.30 9-bit interface

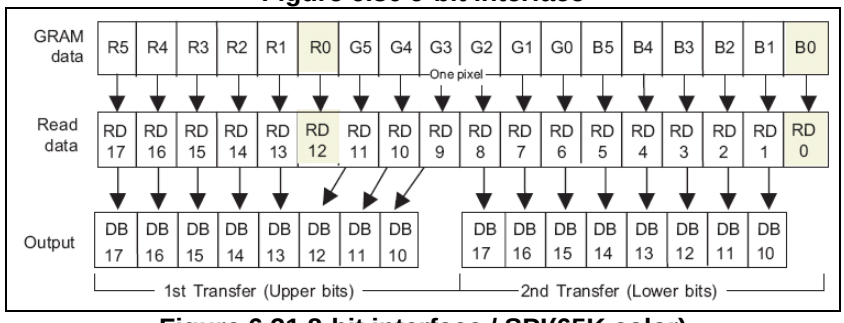


Figure 6.31 8-bit interface / SPI(65K color)

6.2.22. Power Control 7 (R29h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

VCM [5:0]: These pins are to set the factor for generating VCOMH.

Table 6-24 summarized the factor of VERG1OUT

Table 6-24

VCM[5:0]	VCOMH voltage
6'h00	VREG1OUT x 0.685
6'h01	VREG1OUT x 0.690
6'h02	VREG1OUT x 0.695
6'h03	VREG1OUT x 0.700
6'h04	VREG1OUT x 0.705
6'h05	VREG1OUT x 0.710
6'h06	VREG1OUT x 0.715
6'h07	VREG1OUT x 0.720
6'h08	VREG1OUT x 0.725
6'h09	VREG1OUT x 0.730
6'h0A	VREG1OUT x 0.735
6'h0B	VREG1OUT x 0.740
6'h0C	VREG1OUT x 0.745
6'h0D	VREG1OUT x 0.750
6'h0E	VREG1OUT x 0.755
6'h0F	VREG1OUT x 0.760
6'h10	VREG1OUT x 0.765
6'h11	VREG1OUT x 0.770
6'h12	VREG1OUT x 0.775
6'h13	VREG1OUT x 0.780
6'h14	VREG1OUT x 0.785
6'h15	VREG1OUT x 0.790
6'h16	VREG1OUT x 0.795
6'h17	VREG1OUT x 0.800
6'h18	VREG1OUT x 0.805
6'h19	VREG1OUT x 0.810
6'h1A	VREG1OUT x 0.815
6'h1B	VREG1OUT x 0.820
6'h1C	VREG1OUT x 0.825
6'h1D	VREG1OUT x 0.830
6'h1E	VREG1OUT x 0.835
6'h1F	VREG1OUT x 0.840

VCM[5:0]	VCOMH voltage
6'h20	VREG1OUT x 0.845
6'h21	VREG1OUT x 0.850
6'h22	VREG1OUT x 0.855
6'h23	VREG1OUT x 0.860
6'h24	VREG1OUT x 0.865
6'h25	VREG1OUT x 0.870
6'h26	VREG1OUT x 0.875
6'h27	VREG1OUT x 0.880
6'h28	VREG1OUT x 0.885
6'h29	VREG1OUT x 0.890
6'h2A	VREG1OUT x 0.895
6'h2B	VREG1OUT x 0.900
6'h2C	VREG1OUT x 0.905
6'h2D	VREG1OUT x 0.910
6'h2E	VREG1OUT x 0.915
6'h2F	VREG1OUT x 0.920
6'h30	VREG1OUT x 0.925
6'h31	VREG1OUT x 0.930
6'h32	VREG1OUT x 0.935
6'h33	VREG1OUT x 0.940
6'h34	VREG1OUT x 0.945
6'h35	VREG1OUT x 0.950
6'h36	VREG1OUT x 0.955
6'h37	VREG1OUT x 0.960
6'h38	VREG1OUT x 0.965
6'h39	VREG1OUT x 0.970
6'h3A	VREG1OUT x 0.975
6'h3B	VREG1OUT x 0.980
6'h3C	VREG1OUT x 0.985
6'h3D	VREG1OUT x 0.990
6'h3E	VREG1OUT x 0.995
6'h3F	VREG1OUT x 0.1000

6.2.23. Frame rate control (R2Bh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS3	FRS2	FRS1	FRS0

FRS[4:0] Set the oscillator frequency to change frame rate.

Table 6-25 summarized the oscillator frequency and the frame rate.

Note 1: The frame rate is relative to DIVI[1:0] ; RTNI[4:0] ; NL[5:0] ; BP[3:0] and FP[3:0] bits.

Table 6-25

FRS[3:0]	OSC frequency	Frame rate
6'h00	157K	30 Hz
6'h01	163K	31 Hz
6'h02	174K	33 Hz
6'h03	184K	35 Hz
6'h04	200K	38 Hz
6'h05	211K	40 Hz
6'h06	226K	43 Hz
6'h07	247K	47 Hz

FRS[3:0]	OSC frequency	Frame rate
6'h08	268K	51 Hz
6'h09	295K	56 Hz
6'h0A	326K	62 Hz
6'h0B	368K	70 Hz
6'h0C	421K	80 Hz
6'h0D	490K	93 Hz
6'h0E	589K	112 Hz
6'h0F	589K	112 Hz

Formula to calculate frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per line} \times \text{division ratio} \times (\text{Line} + \text{BP} + \text{FP})} \quad [\text{Hz}]$$

fosc: frequency of RC oscillator (FRS bits)

Line: number of lines for driving liquid crystal (NL bits)

Division ratio: DIVI bits

Clock cycles per line: RTNI bits

FP: the number of lines for the front porch period (FP bits)

BP: the number of lines for the back porch period (BP bits)

6.2.24. γ Control (R30h to R3Dh)

	R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R30	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
R31	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
R32	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
R35	W	1	0	0	0	0	0	RP1[2]	RP1[2]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[2]	RP0[0]
R36	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R37	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
R38	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
R39	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
R3C	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
R3D	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

γ **Control (R30h to R3Dh):** OTM3225A provides 10 gamma registers to fine tune gamma output voltage.

KP5-0[2:0]: γ **fine tune** registers for positive polarity.
RP1-0[2:0]: γ **gradient** registers for positive polarity.
VRP1-0[4:0]: γ **amplitude** registers for positive polarity.
KN5-0[2:0]: γ **fine tune** registers for positive polarity.
RN1-0[2:0]: γ **gradient** registers for positive polarity.
VRN1-0[4:0]: γ **amplitude** registers for positive polarity.

6.2.25. Window Horizontal RAM Address Start (R50h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0

6.2.26. Window Horizontal RAM Address End (R51h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0

6.2.27. Window Vertical RAM Address Start (R52h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

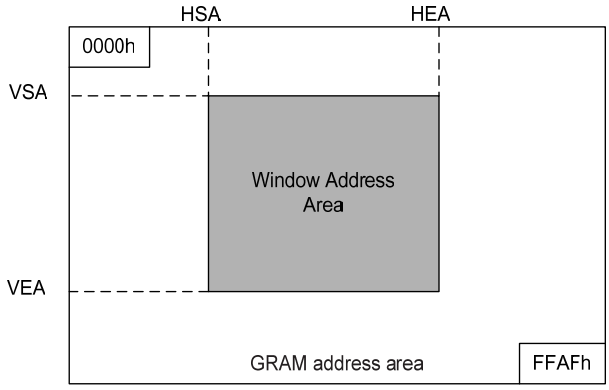
6.2.28. Window Vertical RAM Address End (R53h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0

HSA7-0/HEA7-0: OTM3225A provides window access function. Set HSA7-0 and HEA7-0 represent the start address and end address of the window function in horizontal direction. To use window-accessing function, HSA and HEA bits must be set before starting RAM write operation. Be aware that “00”h ≤ HSA7-0< HEA7-0 ≤ “EF”h and HEA-HSA>=”01h”.

VSA8-0/VEA8-0: OTM3225A provides window access function. Set VSA8-0 and VEA8-0 represent the start address and end address of the window in vertical direction. To use window accessing function, VSA and VEA bits must be set before starting RAM write operation. Be aware that “00”h ≤ VSA8-0< VEA8-0 ≤ 9’h13F.

Figure 6.32 illustrates the window-accessing function using R50h~R53h.



6.2.29. Gate Driver Scan Control (R60h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

SCN5-0: Set the SCN5-0 bits can specify the starting position of the gate driver. The start position of gate driver is determined by the combination of the setting of GS and SM.

Table 6-26 summarized the starting position for each SCN5-0 setting.

Table 6-26

SCN[5:0]	Scan Start Position (Gate line)			
	SM=0		SM=1	
	GS = "0"	GS = "1"	GS = "0"	GS = "1"
6'h00	G1	G320	G1	G320
6'h01	G9	G312	G17	G304
6'h02	G17	G304	G33	G288
6'h03	G25	G296	G49	G272
6'h04	G33	G288	G65	G256
6'h05	G41	G280	G81	G240
6'h06	G49	G272	G97	G224
6'h07	G57	G264	G113	G208
6'h08	G65	G256	G129	G192
6'h09	G73	G248	G145	G176
6'h0A	G81	G240	G161	G160
6'h0B	G89	G232	G177	G144
6'h0C	G97	G224	G193	G128
6'h0D	G105	G216	G209	G112
6'h0E	G113	G208	G2	G96
6'h0F	G121	G200	G18	G80
6'h10	G129	G192	G34	G64
6'h11	G137	G184	G50	G48
6'h12	G145	G176	G66	G32
6'h13	G153	G168	G82	G16
6'h14	G161	G160	G98	G319
6'h15	G169	G152	G114	G303
6'h16	G177	G144	G130	G287
6'h17	G185	G136	G146	G271
6'h18	G193	G128	G162	G255
6'h19	G201	G120	G178	G239
6'h1A	G209	G112	G194	G223
6'h1B	G217	G104	G114	G207
6'h1C	G225	G96	G130	G191
6'h1D	G233	G88	G146	G175
6'h1E	G241	G80	G162	G159
6'h1F	G249	G72	G178	G143
6'h20	G257	G64	G194	G127
6'h21	G265	G56	G210	G111
6'h22	G273	G48	G226	G95
6'h23	G281	G40	G242	G79
6'h24	G289	G32	G258	G63
6'h25	G297	G24	G274	G47
6'h26	G305	G16	G290	G31
6'h27	G313	G8	G306	G15
6'h28~3F	Setting disabled			

NL5-0: Set the number of gate lines for different resolution of display panel. The combination of NL5-NL0 represents the gate line number are summarized at **Table 6-27**.

Table 6-27

NL[5:0]	Display Size	Drive lines
6'h00	720 x 8 dots	8
6'h01	720 x 16 dots	16
6'h02	720 x 24 dots	24
…	…	…
6'h1F	720 x 256 dots	256
6'h20	720 x 264 dots	264
6'h21	720 x 272 dots	272
6'h22	720 x 280 dots	280
6'h23	720 x 288 dots	288
6'h24	720 x 296 dots	296
6'h25	720 x 304 dots	304
6'h26	720 x 312 dots	312
6'h27	720 x 320 dots	320

Note 1: Be sure that NL[5:0]≧SCN[5:0].

Note 2: Be sure that NL[5:0]≦6'h27.

GS: Shift direction of the gate driver output selection. When
GS="0", gate driver shift from G1 to G320. When GS = "1", gate driver shift from G320 to G1.

6.2.30. Driver Output Control (R61h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV

REV: To set the grayscale corresponding to normally white or normally black LCD panel from same data input.

Table 6-2812**Table 6-28** summarized REV bit function.

Table 6-28

REV	GRAM data	Source Driver Output	
		Positive Polarity	Negative Polarity
0	18'h00000 ⋮ 18'h3FFFF	V63 ⋮ V0	V0 ⋮ V63
1	18'h00000 ⋮ 18'h3FFFF	V0 ⋮ V63	V63 ⋮ V0

VLE: OTM3225A provides vertical scrolling function which can be set by VLE bit.

VLE = "1", vertical scrolling function enable. The amount of scrolling line from the first line is determined by VL[8:0].

VLE = "0", normal display.

NDL: set the source diver output level in non-lit area..

NDL = "1", .

NDL = "0", .

6.2.31. Vertical Scroll Control (R6Ah)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL8-0: OTM3225A provides scrolling function. The start position for displaying the image is shifted vertically by the number of lines based on the setting of the VL8-0 bits. Be aware that the vertical scrolling function is not available in the external (RGB) display interface mode. **Table 6-29** summarized the function of VL8-0 setting.

Table 6-29

VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling lines
0	0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	1	0	2 lines
	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	1	1	319 lines
1	0	1	0	0	0	0	0	0	320 lines

Note 1: Be sure that VL[8:0]≦9'h140.

6.2.32. Display Position – Partial Display 1 (R80h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00

6.2.33. RAM Address Start – Partial Display 1 (R81h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00

6.2.34. RAM Address End – Partial Display 1 (R82h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00

6.2.35. Display Position – Partial Display 2 (R83h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10

6.2.36. RAM Address Start – Partial Display 2 (R84h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10

6.2.37. RAM Address End – Partial Display 2 (R85h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10

PTDP0[8:0]: Set the physical starting position of partial display 1 on the LCD panel

PTDP1[8:0]: Set the physical starting position of partial display 2 on the LCD panel

The partial display 1 and partial display 2 should not overlap with each other. And make sure the PTDP0[8:0] < PTDP1[8:0].

PTSA0[8:0]: Set the start line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

PTEA0[8:0]: Set the end line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

Note 1: Make sure PTSA0<=PTEA0

PTSA1[8:0]: Set the start line address of display RAM of partial display2 which will be display according to PTDP1[8:0].

PTEA1[8:0]: Set the end line address of display RAM of partial display2 which will be display according to PTDP1[8:0]

Note 1: Make sure PTSA1<=PTEA1

6.2.38. Panel Interface Control 1 (R90h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI 3	RTNI 2	RTNI 1	RTNI 0

RTNI4-0: Set the clock cycle per line **Table 6-30** summarized the function of RTNI4-0 setting.

Table 6-30

RTNI4	RTNI3	RTNI2	RTNI1	RTNI0	Clock Cycles per line
0	0	0	0	0	16 clocks
0	0	0	0	1	17 clocks
0	0	0	1	0	18 clocks
0	0	0	1	1	19 clocks
0	0	1	0	0	20 clocks
0	0	1	0	1	21 clocks
0	0	1	1	0	22 clocks
0	0	1	1	1	23 clocks
0	1	0	0	0	24 clocks
0	1	0	0	1	25 clocks
0	1	0	1	0	26 clocks
0	1	0	1	1	27 clocks
0	1	1	0	0	28 clocks
0	1	1	0	1	29 clocks
0	1	1	1	0	30 clocks
0	1	1	1	1	31 clocks
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

DIVI1-0: To specified the division ratio of internal operation clock frequency. Set the RTN and DIVI bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIVI1-0 bits are disabled. **Table 6-31** summarized the function of DIVI1-0 setting.

Table 6-31

DIVI1	DIVI0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

6.2.39. Panel Interface Control 2 (R92h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0

NOWI [2:0]: Set the adjacent gate driver output non-overlap period. **Table 6-32** summarized the function of NOWI2-0 setting.

Table 6-32

NOWI2	NOWI1	NOWI0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	1 clock
0	0	1	1 clocks
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	4 clocks
1	0	1	5 clocks
1	1	0	6 clocks
1	1	1	7 clocks

6.2.40. Panel Interface control 4 (R95h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0

RTNE5-0: Set the clock cycle per line **Table 6-33** summarized the function of RTNE5-0 setting.

Table 6-33

RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Clock Cycles per line
0	1/0	0	0	0	0	16 clocks
0	1/0	0	0	0	1	17 clocks
0	1/0	0	0	1	0	18 clocks
0	1/0	0	0	1	1	19 clocks
0	1/0	0	1	0	0	20 clocks
0	1/0	0	1	0	1	21 clocks
0	1/0	0	1	1	0	22 clocks
0	1/0	0	1	1	1	23 clocks
0	1/0	1	0	0	0	24 clocks
0	1/0	1	0	0	1	25 clocks
0	1/0	1	0	1	0	26 clocks
0	1/0	1	0	1	1	27 clocks
0	1/0	1	1	0	0	28 clocks
0	1/0	1	1	0	1	29 clocks
0	1/0	1	1	1	0	30 clocks
0	1/0	1	1	1	1	31 clocks
1	1	0	0	0	0	32 clocks
1	1	0	0	0	1	33 clocks
1	1	0	0	1	0	34 clocks
1	1	0	0	1	1	35 clocks
1	1	0	1	0	0	36 clocks
1	1	0	1	0	1	37 clocks
1	1	0	1	1	0	38 clocks
1	1	0	1	1	1	39 clocks
1	1	1	0	0	0	40 clocks
1	1	1	0	0	1	41 clocks
1	1	1	0	1	0	42 clocks
1	1	1	0	1	1	43 clocks
1	1	1	1	0	0	44 clocks
1	1	1	1	0	1	45 clocks
1	1	1	1	1	0	46 clocks
1	1	1	1	1	1	47 clocks
1	1	0	0	0	0	48 clocks
1	1	0	0	0	1	49 clocks
1	1	0	0	1	0	50 clocks
1	1	0	0	1	1	51 clocks
1	1	0	1	0	0	52 clocks

RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Clock Cycles per line
1	1	0	1	0	1	53 clocks
1	1	0	1	1	0	54 clocks
1	1	0	1	1	1	55 clocks
1	1	1	0	0	0	56 clocks
1	1	1	0	0	1	57 clocks
1	1	1	0	1	0	58 clocks
1	1	1	0	1	1	59 clocks
1	1	1	1	0	0	60 clocks
1	1	1	1	0	1	61 clocks
1	1	1	1	1	0	62 clocks
1	1	1	1	1	1	63 clocks

DIVE1-0: To specified the division ratio of internal operation clock frequency. Set the RTNE and DIVE bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIVE1-0 bits are disabled. **Table 6-34** summarized the function of DIVE1-0 setting.

Table 6-34

DIVE1	DIVE0	Division Ratio	Internal Operation Clock Frequency
0	0	4	fosc / 4
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc =Frequency of RC oscillation

6.2.41. Panel Interface Control 5 (R97h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0

NOWE [3:0]: Set the adjacent gate driver output non-overlap period in RGB interface. **Table 6-35** summarized the function of NOWE3-0 setting.

Table 6-35

NOWE3	NOWE2	NOWE1	NOWE0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	0	1 clock
0	0	0	1	2 clocks
0	0	1	0	3 clocks
0	0	1	1	4 clocks
0	1	0	0	5 clocks
0	1	0	1	6 clocks
0	1	1	0	7 clocks
0	1	1	1	8 clocks
1	0	0	0	9 clocks
1	0	0	1	10 clocks
1	0	1	0	11 clocks
1	0	1	1	12 clocks
1	1	0	0	13 clocks
1	1	0	1	14 clocks
1	1	1	0	15 clocks
1	1	1	1	15 clocks

7. GRAM

Table 7-1 GRAM address and display panel position (SS = “0”)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	….	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			….	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G320	“00000"H			“00001"H			“00002"H			"00003"H			….	"000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G319	"00100"H			"00101"H			"00102"H			"00103"H			….	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G318	"00200"H			"00201"H			"00202"H			"00203"H			….	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G317	"00300"H			"00301"H			"00302"H			"00303"H			….	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G316	"00400"H			"00401"H			"00402"H			"00403"H			….	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
G6	G315	"00500"H			"00501"H			"00502"H			"00503"H			….	"005EC"H			"005ED"H			"005EE"H			"005EF"H		
G7	G314	"00600"H			"00601"H			"00602"H			"00603"H			….	"006EC"H			"06ED"H			"06EE"H			"06EF"H		
G8	G313	"00700"H			"00701"H			"00702"H			"00703"H			….	“007EC"H			“007ED"H			“007EE"H			“007EF"H		
G9	G312	“00800"H			“00801"H			“00802"H			“00803"H			….	“008EC"H			“008ED"H			“008EE"H			“008EF"H		
G10	G311	“00900"H			“00901"H			“00902"H			“00903"H			….	“009EC"H			“009ED"H			“009EE"H			“009EF"H		
G11	G310	“00E00"H			“00E01"H			“00E02"H			“00E03"H			….	“00EEC"H			“00EED"H			“00EEE"H			“00EEF"H		
G12	G309	“00B00"H			“00B01"H			“00B02"H			“00B03"H			….	“00BEC"H			“00BED"H			“00BEE"H			“00BEF"H		
G13	G308	“00C00"H			“00C01"H			“00C02"H			“00C03"H			….	“00CEC"H			“00CED"H			“00CEE"H			“00CEF"H		
G14	G307	“00D00"H			“00D01"H			“00D02"H			“00D03"H			….	“00DEC"H			“00DED"H			“00DEE"H			“00DEF"H		
G15	G306	“00E00"H			“00E01"H			“00E02"H			“00E03"H			….	“00EEC"H			“00EED"H			“00EEE"H			“00EEF"H		
G16	G305	“00F00"H			“00F01"H			“00F02"H			“00F03"H			….	“00FEC"H			“00FED"H			“00FEE"H			“00FEF"H		
G17	G304	“01000"H			“01001"H			“01002"H			“01003"H			….	“010EC"H			“010ED"H			“010EE"H			“010EF"H		
G18	G303	“01100"H			“01101"H			“01102"H			“01103"H			….	“011EC"H			“011ED"H			“011EE"H			“011EF"H		
G19	G302	“01200"H			“01201"H			“01202"H			“01203"H			….	“012EC"H			“012ED"H			“012EE"H			“012EF"H		
G20	G301	“01300"H			“01301"H			“01302"H			“01303"H			….	“013EC"H			“013ED"H			“013EE"H			“013EF"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G313	G8	“13800"H			“13801"H			“13802"H			“13803"H			….	“138EC"H			“138ED"H			“138EE"H			“138EF"H		
G314	G7	“13900"H			“13901"H			“13902"H			“13903"H			….	“139EC"H			“139ED"H			“139EE"H			“139EF"H		
G315	G6	“13A00"H			“13A01"H			“13A02"H			“13A03"H			….	“13AEC"H			“13AED"H			“13AEE"H			“13AEF"H		
G316	G5	“13B00"H			“13B01"H			“13B02"H			“13B03"H			….	“13BEC"H			“13BED"H			“13BEE"H			“13BEF"H		
G317	G4	“13C00"H			“13C01"H			“13C02"H			“13C03"H			….	“13CEC"H			“13CED"H			“13CEE"H			“13CEF"H		
G318	G3	“13D00"H			“13D01"H			“13D02"H			“13D03"H			….	“13DEC"H			“13DED"H			“13DEE"H			“13DEF"H		
G319	G2	“13E00"H			“13E01"H			“13E02"H			“13E03"H			….	“13EEC"H			“13EED"H			“13EEE"H			“13EEF"H		
G320	G1	“13F00"H			“13F01"H			“13F02"H			“13F03"H			….	“13FEC"H			“13FED"H			“13FEE"H			“13FEF"H		

Table 7-2 GRAM address and display panel position (SS = "1")

S/G pin		S1	S2	S3	S4	S5	…	S7	S8	S9	S10	S11	S12	….	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			….	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G320	"000EF"H			"000EE"H			"000ED"H			"000EC"H			….	"00003"H			"00002"H			"00001"H			"00000"H		
G2	G319	"001EF"H			"001EE"H			"001ED"H			"001EC"H			….	"00103"H			"00102"H			"00101"H			"00100"H		
G3	G318	"002EF"H			"002AE"H			"002ED"H			"002EC"H			….	"00203"H			"00202"H			"00201"H			"00200"H		
G4	G317	"003EF"H			"003EE"H			"003ED"H			"003EC"H			….	"00303"H			"00302"H			"00301"H			"00300"H		
G5	G316	"004EF"H			"004EE"H			"004ED"H			"004EC"H			….	"00403"H			"00402"H			"00401"H			"00400"H		
G6	G315	"005EF"H			"005EE"H			"005ED"H			"005EC"H			….	"00503"H			"00502"H			"00501"H			"00500"H		
G7	G314	"006EF"H			"006EE"H			"006ED"H			"006EC"H			….	"00603"H			"00602"H			"00601"H			"00600"H		
G8	G313	"007EF"H			"007EE"H			"007ED"H			"007EC"H			….	"00703"H			"00702"H			"00701"H			"00700"H		
G9	G312	"008EF"H			"008EE"H			"008ED"H			"008EC"H			….	"00803"H			"00802"H			"00801"H			"00800"H		
G10	G311	"009EF"H			"009EE"H			"009ED"H			"009EC"H			….	"00903"H			"00902"H			"00901"H			"00900"H		
G11	G310	"00AEF"H			"00AEE"H			"00AED"H			"00AEC"H			….	"00E03"H			"00A02"H			"00A01"H			"00A00"H		
G12	G309	"00BEF"H			"00BEE"H			"00BED"H			"00BEC"H			….	"00B03"H			"00B02"H			"00B01"H			"00B00"H		
G13	G308	"00CEF"H			"00CEE"H			"00CED"H			"00CEC"H			….	"00C03"H			"00C02"H			"00C01"H			"00C00"H		
G14	G307	"00DEF"H			"00DEE"H			"00DED"H			"00DEC"H			….	"00D03"H			"00D02"H			"00D01"H			"00D00"H		
G15	G306	"00EEF"H			"00EEE"H			"00EED"H			"00EEC"H			….	"00E03"H			"00E02"H			"00E01"H			"00E00"H		
G16	G305	"00FEF"H			"00FEE"H			"00FED"H			"00FEC"H			….	"00F03"H			"00F02"H			"00F01"H			"00F00"H		
G17	G304	"010EF"H			"010EE"H			"010ED"H			"010EC"H			….	"01003"H			"01002"H			"01001"H			"01000"H		
G18	G303	"011EF"H			"011EE"H			"011ED"H			"011EC"H			….	"01103"H			"01102"H			"01101"H			"01100"H		
G19	G302	"012EF"H			"012EE"H			"012ED"H			"012EC"H			….	"01203"H			"01202"H			"01201"H			"01200"H		
G20	G301	"013EF"H			"013EE"H			"013ED"H			"013EC"H			….	"01303"H			"01302"H			"01301"H			"01300"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G233	G8	"E8EF"H			"138EE"H			"138ED"H			"138EC"H			….	"13803"H			"13802"H			"13801"H			"13800"H		
G234	G7	"139EF"H			"139EE"H			"139ED"H			"139EC"H			….	"13903"H			"13902"H			"13901"H			"13900"H		
G235	G6	"13AEF"H			"13AEE"H			"13AED"H			"13AEC"H			….	"13A03"H			"13A02"H			"13A01"H			"13A00"H		
G236	G5	"13BEF"H			"13BEE"H			"13BED"H			"13BEC"H			….	"13B03"H			"13B02"H			"13B01"H			"13B00"H		
G237	G4	"13CEF"H			"13CEE"H			"13CED"H			"13CEC"H			….	"13C03"H			"13C02"H			"13C01"H			"13C00"H		
G238	G3	"13DEF"H			"13DEE"H			"13DED"H			"13DEC"H			….	"13D03"H			"13D02"H			"13D01"H			"13D00"H		
G239	G2	"13EEF"H			"13EEE"H			"13EED"H			"13EEC"H			….	"13E03"H			"13E02"H			"13E01"H			"13E00"H		
G240	G1	"13FEF"H			"13FEE"H			"13FED"H			"13FEC"H			….	"13F03"H			"13F02"H			"13F01"H			"13F00"H		

8. INTERFACES

The OTM3225A provides different interfaces to meet the diverse need of small/medium size LCD. Based on the application requirement, there are three different display modes which are most used in end product.

1. Still picture display
2. Moving picture display.
3. Re-writing still pictures while moving picture are display.

For above three different display requirements, OTM3225A provides different interfaces to meet the requirement.

1. System interface
2. External interface (RGB interface)
3. VSYNC interface

System interface is suitable for still picture display while RGB interface and VSYNC interface are suitable for moving picture display. Be aware that RGB or VSYNC interface still can used to display still picture and system interface can also display moving picture. **Table 8-1** summarized different interfaces for different display requirement.

Table 8-1

Display State	Operation Mode	RAM access Mode(RM)	Display operation Mode (DM1-0)
Still pictures	Internal clock	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving pictures	RGB interface	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)
Low Speed moving picture	RGB interface	RGB interface (RM = 1)	Internal clock operation (DM1-0 = 00)

8.1. System Interface

The system interfaces of OTM3225A can support 8-bit, 9-bit, 16-bit, 18-bit 80-system Interface and Serial Peripheral Interface (SPI), which can be set by the IM3/2/1/0 pins. The system interface can set instructions and access RAM. **Table 8-2** summarized the interface corresponding to IM3-0 setting.

Table 8-2

IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use
0	0	0	0	Setting disabled	-
0	0	0	1	Setting disabled	-
0	0	1	0	80-system 16-bit interface	DB17 to 10 and 8 to 1
0	0	1	1	80-system 8-bit interface	DB17 to 10
0	1	0	*/ID	Serial peripheral interface (SPI)	DB1 to 0
0	1	1	0	Setting disabled	-
1	0	0	0	Setting disabled	-
1	0	0	1	Setting disabled	-
1	0	1	0	80-system 18-bit interface	DB17 to 0
1	0	1	1	80-system 9-bit interface	DB17 to 9
1	1	*	*	Setting disabled -	-

8.1.1. 80-system 18-bit interface

The instruction and GRAM accessing format of 80-system 18-bit interface are shown in **Figure 8-1** and **Figure 8-2**, respectively.

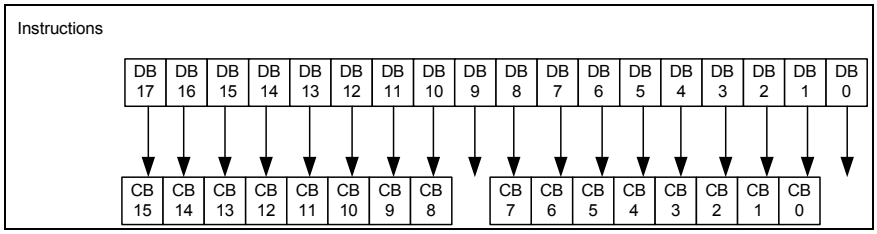


Figure 8-1

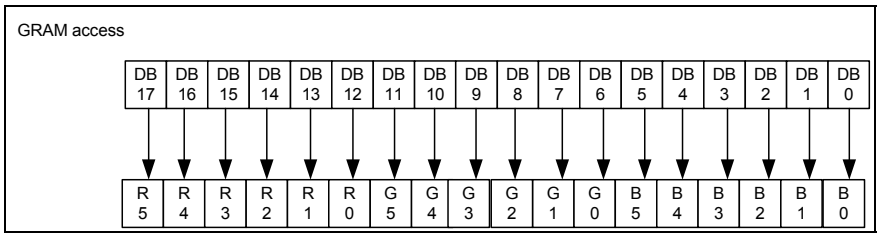


Figure 8-2

8.1.2. 80-system 16-bit interface

The instruction and GRAM accessing format of 80-system 16-bit interface are shown in **Figure 8-3** and **Figure 8-4**, respectively.

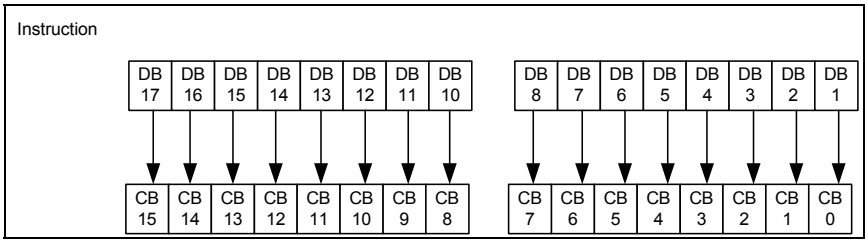


Figure 8-3

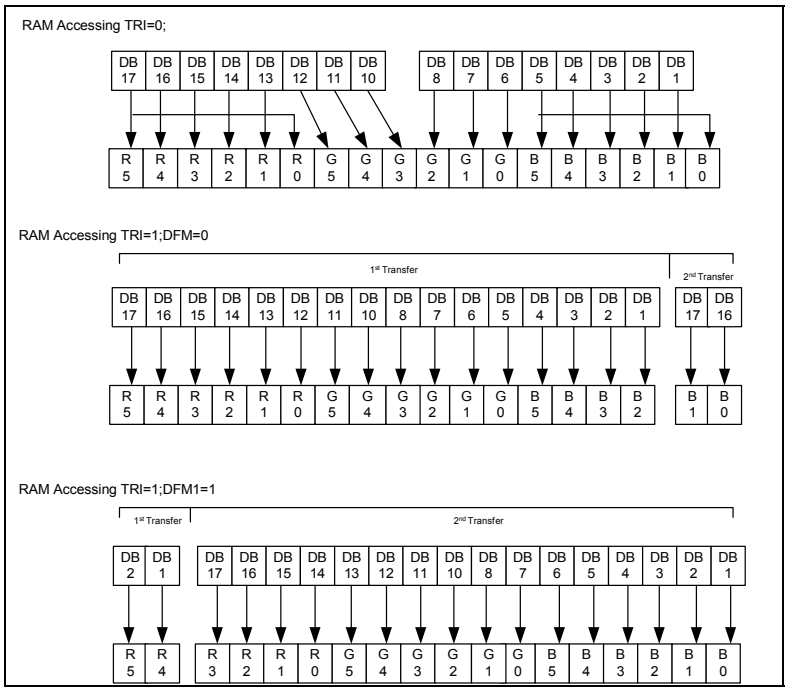


Figure 8-4

8.1.3. 80-system 9-bit interface

The instruction and GRAM accessing format of 80-system 9-bit interface are shown in **Figure 8-5** and **Figure 8-6**, respectively.

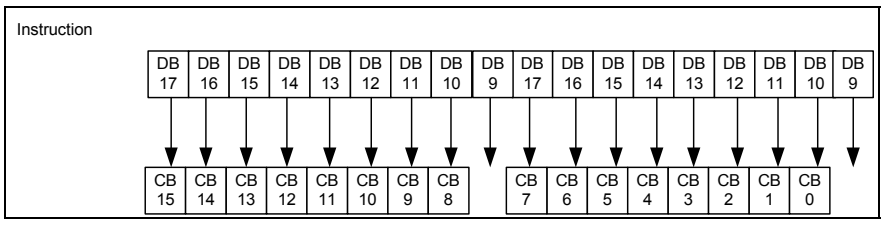


Figure 8-5

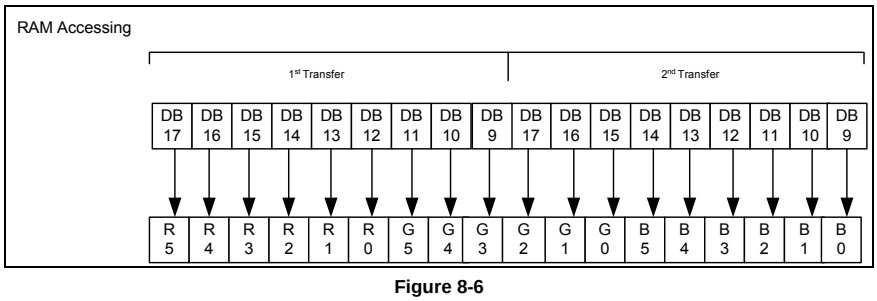


Figure 8-6

8.1.4. 80-system 8-bit interface

The instruction and GRAM accessing format of 80-system 8-bit interface are shown in **Figure 8-7** and **Figure 8-8**, respectively.

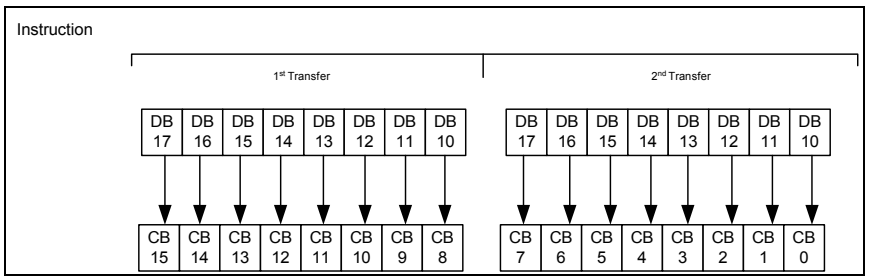


Figure 8-7

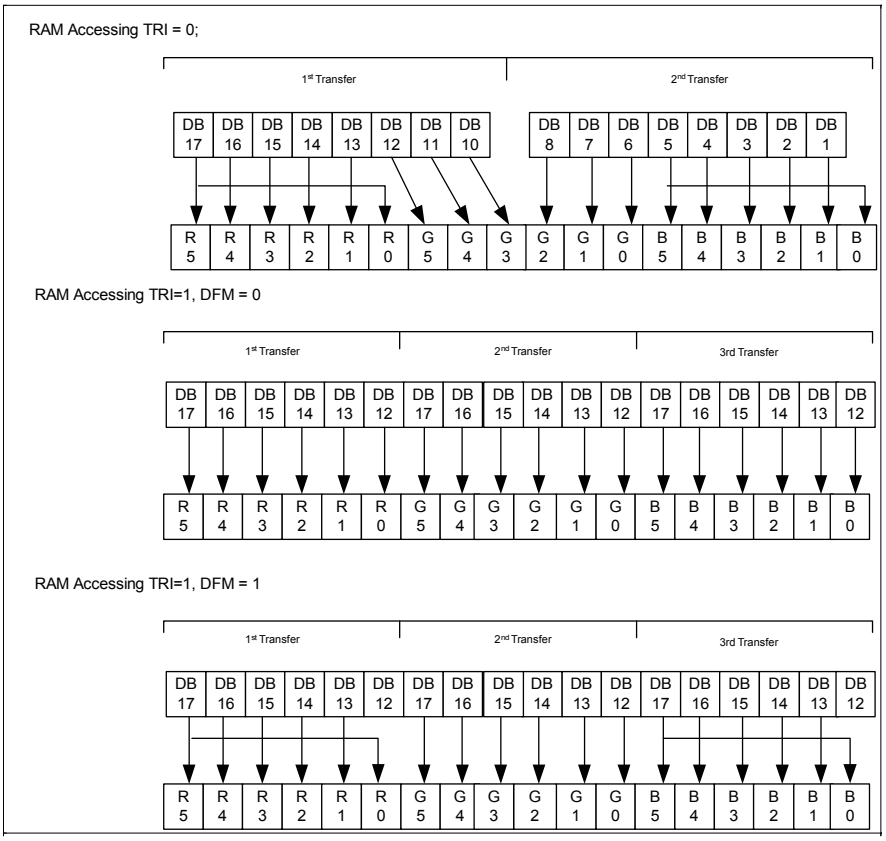


Figure 8-8

8.1.5. Serial Peripheral interface (SPI)

The system interface of OTM3225A also includes the Serial Peripheral Interface (SPI). In SPI mode, /CS, SCL, SDI and SDO are used to transfer data between MCU and OTM3225A. IM0/ID pin served as the ID pin. **Figure 8-9** illustrates the detail timing while using SPI. Be aware that the unused pins such as DB17-0 pins must be fixed at either IOVCC or GND level.

The instruction and GRAM accessing format of SPI interface are shown in **Figure 8-10** and **Figure 8-11**, respectively.
When read operation is desired In SPI mode, valid data are read out as the OTM3225A reads out the 6th byte data from the internal GRAM. The RAM data transfer in SPI mode, in SPI mode with status read are illustrated in **Figure 8-12**, , respectively.

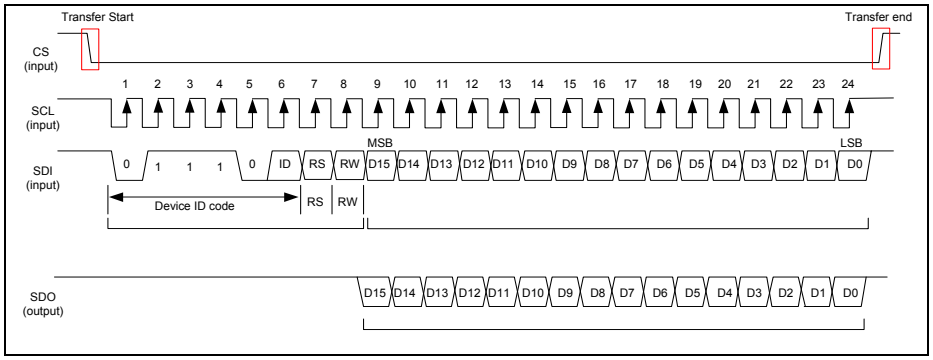


Figure 8-9

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note 1) ID bit is selected by setting the IM0/ID pin.

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

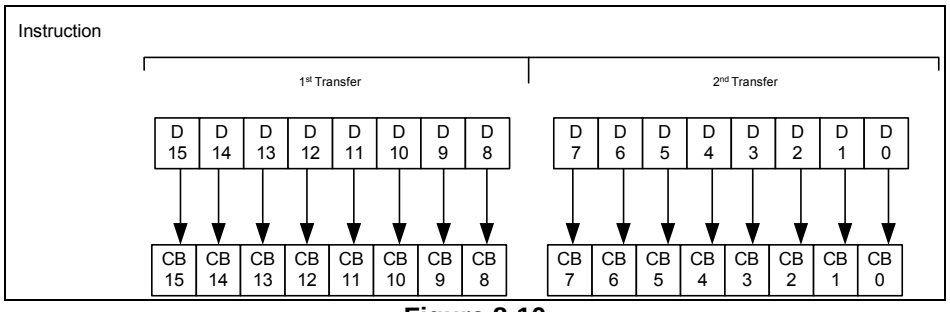


Figure 8-10

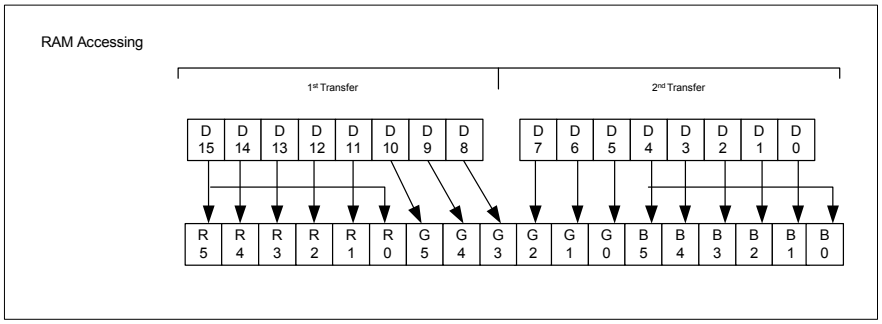


Figure 8-11

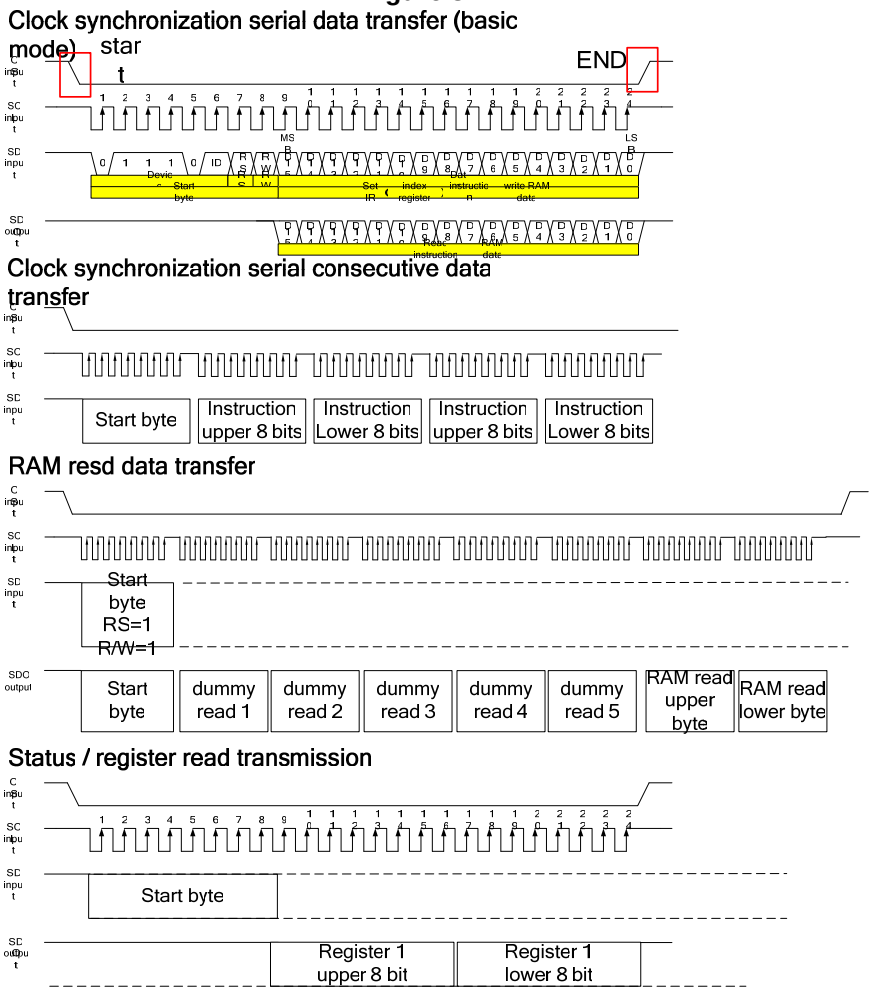


Figure 8-12

8.2. VSYNC Interface

The OTM3225A also supports VSYNC interface for moving picture display, which is the system interface in synchronization with the frame-synchronizing signal (VSYNC). The VSYNC interface can display a moving picture without tremendous modification.

DM1-0 = “10” and RM = “0” can initialized VSYNC interface. In VSYNC interface mode, the internal display operation is synchronized with the VSYNC signal. In VSYNC interface mode, the graphic data are stored in GRAM to minimize the data transfer to overwrite on the moving picture GRAM area. **Figure 8-13** illustrates moving picture data transfer through VSYNC interface.

In VSYNC mode, Internal operation is executed in synchronization with the internal clock generated from internal oscillators and VSYNC input. Therefore the frame rate is determined by the frequency of VSYNC. OTM3225A can access the internal RAM in high speed with less power consumption in VSYNC interface mode while using high-speed write mode

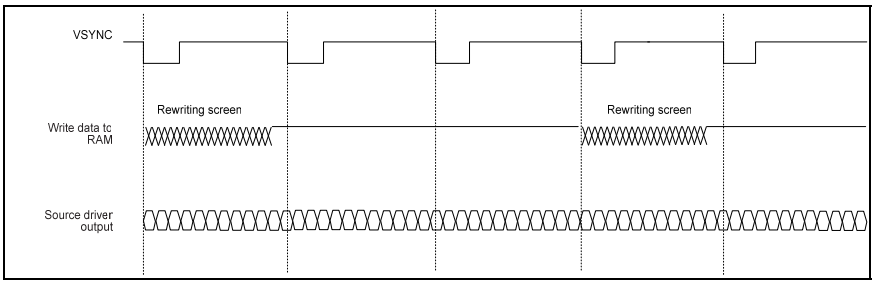


Figure 8-13

In VSYNC interface mode, the formula for Internal clock frequency and frame rate is shown below:

Input clock frequency = FrameRate x (DisplayLines) + FrontPorch + BackPorch x 16 x variance

Due to the possible cause of variances while set the internal clock frequency; be sure to complete the display operation in one VSYNC cycle.

8.3. External Display Interface

OTM3225A also includes external (RGB) interface for displaying moving picture. External interface can be set by RIM1-0 bit. **Table 8-3** summarized the corresponding types of RGB interface with RIM1-0 setting.

Table 8-3

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, 11-1
1	0	6-bit RGB interface	DB17-12
1	1	8-bit RGB interface	DB17-10

RGB interface cab access OTM3225A by VSYNC, HSYNC, ENABLE, DOTCLK and DB17-0 signals, where VSYNC is used for frame synchronization; HSYNC is used for line synchronization and ENABLE is served as the valid data synchronized signals. The RGB interface can be rewriting minimum necessary data to the GRAM area which need to be overwritten with use of window address function and high-speed write mode. It is necessary for RGB interface to set front and back porch periods after and before a display period, respectively. **Figure 8-14** illustrates the general timing for RGB interface. There are some constrain while using RGB interface. The following summarized the conditions

(a) Partial display/ scroll function / interlace and graphics operation function are not available for RGB interface

(b) In RGB interface VSYNC, HSYNC, and DOTCLK signals must be input through a display operation period.

(c) The setting of the NO1-0 bits, STD1-0 bits and EQ1-0 bits are based on DOTCLK in RGB interface mode. In 6-bit RGB interface mode, it takes 3 DOTCLK inputs to transfer one pixel. Be aware data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode is necessary. Set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC ENABLE, DB17-0) to input 3x clock to complete data transfer in units of pixels.

(d) In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

(e) In RGB interface mode, a GRAM address (DB17-0) is set in the address counter every frame on the falling edge of VSYNC.

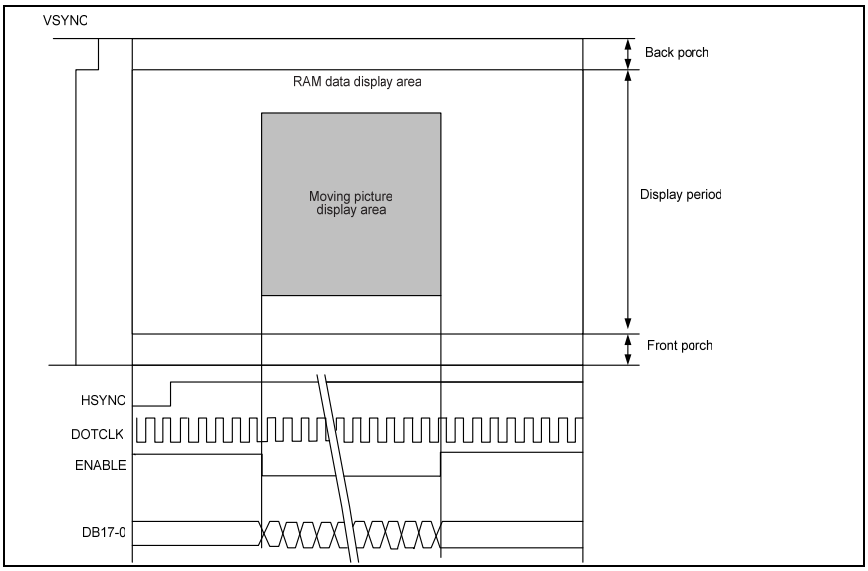


Figure 8-14

RGB interface includes ENABLE signal served as valid data synchronized signals. Moreover, the active level for ENABLE can be set by EPL. The EPL bit inverts the polarity of ENABLE signal. **Table 8-4** summarized the setting of EPL and ENABLE active level for GRAM accessing. Setting both EPL and ENABLE bits to automatically update RAM address in the AC is necessary while writing data to the GRAM.

Table 8-4

EPL	ENABLE	RAM Write	RAM Address
0	0	Enabled	Updated
0	1	Disabled	Retained
1	0	Disabled	Retained
1	1	Enabled	Updated

OTM3225A can support 18-bit, 16-bit , 8-bit and 6-bit RGB interface. The detail timing diagram for 18-bit, 16-bit and 6-bit RGB interface are shown in **Figure 8-15** and **Figure 8-16** respectively.

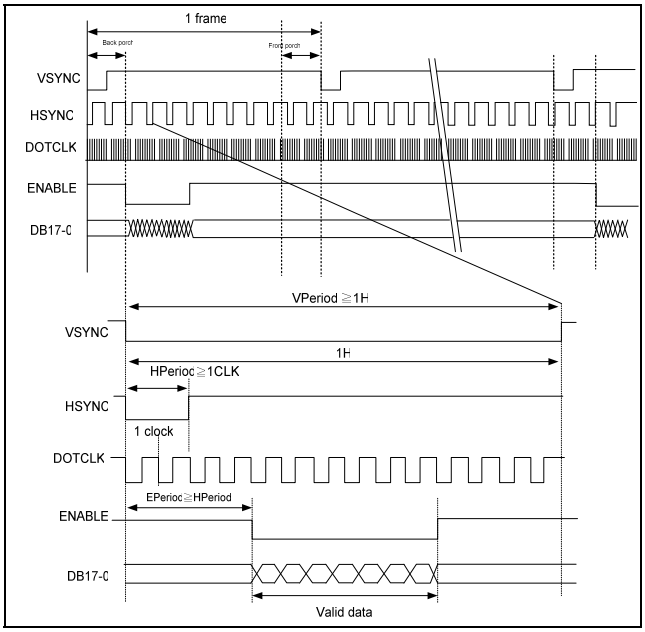


Figure 8-15

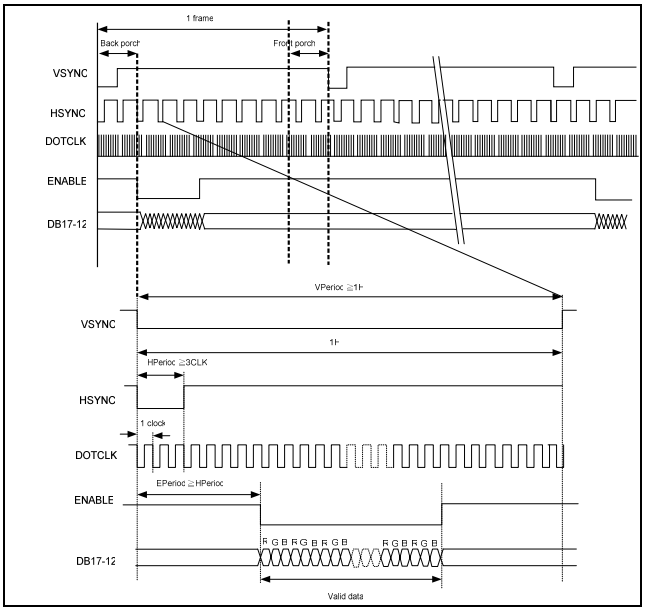


Figure 8-16

The RGB interface also has the window address function to transfer only minimum necessary data on the moving picture GRAM area, which can lower the power consumption and still can use system interface to rewrite data in still picture RAM area while displaying a moving picture. Setting RM = 0 while in RGB interface mode can make GRAM access through the system interface. When RGB interface accessing GRAM is desired, wait for one read/write bus cycle following by RM = 1 setting.

Figure 8-17 illustrates the timing diagram when displaying a moving picture through the RGB interface and rewriting data in the still picture GRAM area through the system interface.

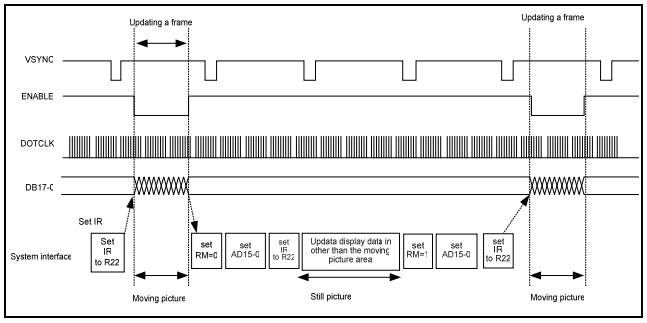


Figure 8-17

8.3.1. 6-bit RGB interface

RAM accessing format and data transmission synchronization of 6-bit RGB interface are shown in **Figure 8-18** and **Figure 8-19**, respectively.

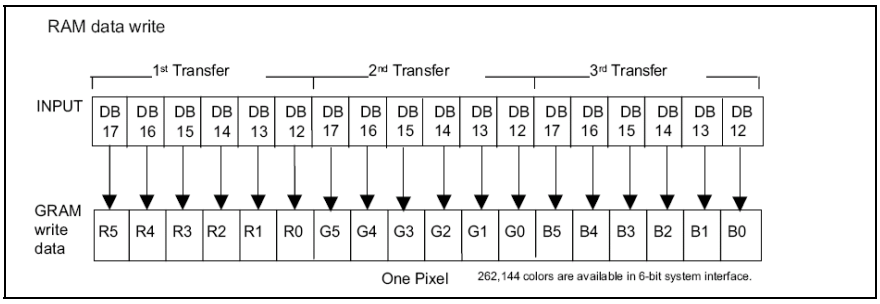


Figure 8-18

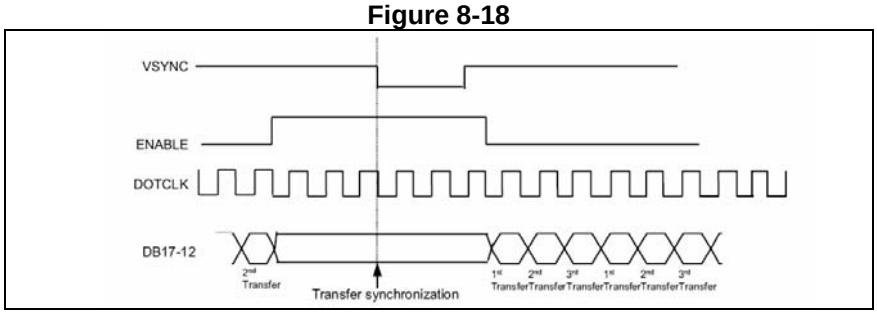


Figure 8-19

8.3.2. 16-bit RGB interface

RAM accessing format of 16-bit RGB interface are shown in **Figure 8-20**.

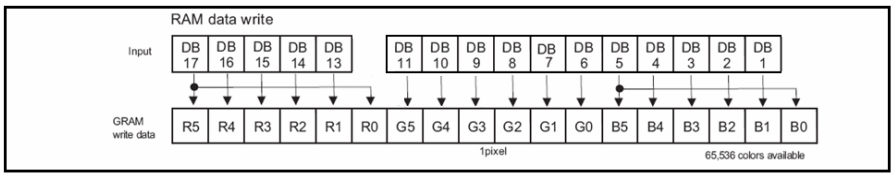


Figure 8-20

8.3.3. 18-bit RGB interface

RAM accessing format of 18-bit RGB interface are shown in **Figure 8-21**.

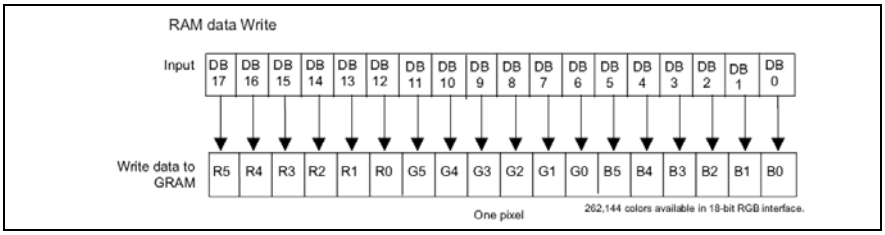
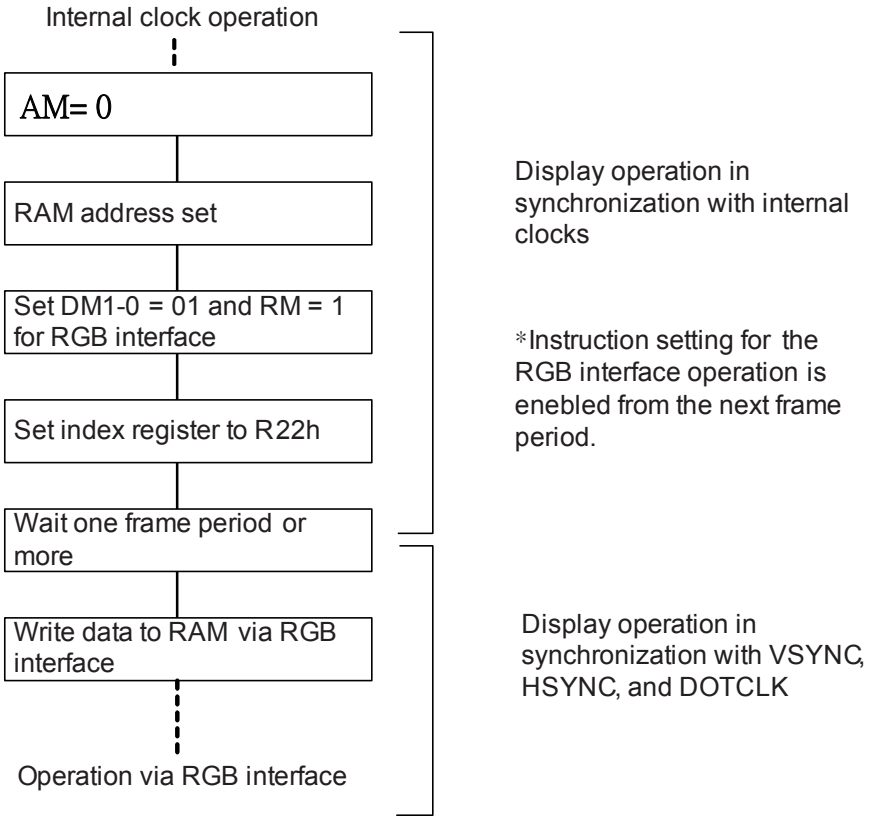


Figure 8-21

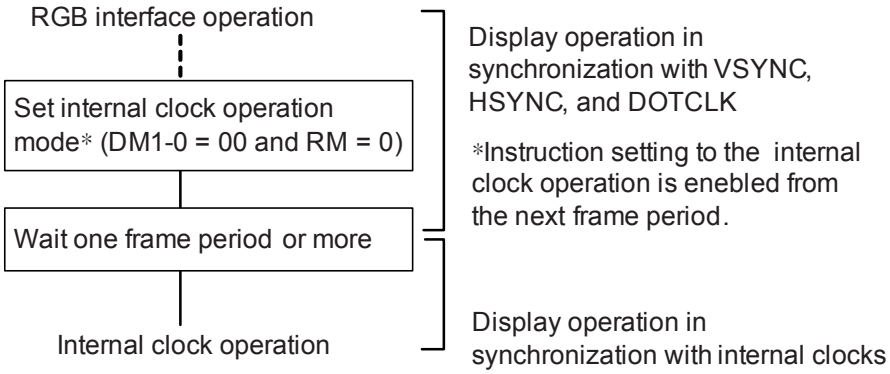
8.4. Sequence to set between system interface and RGB interface:

Internal Clock Operation to RGB Interface (1)



Note: Input the RGB interface signals before setting the DM 1-0 and RM bits to the RGB interface operation.

RGB Interface (1) to Internal Clock Operation



Note: Continue RGB interface signals at least for one frame period after setting DM1-0, RM bits to internal clock operation.

9. Display Feature Function:

9.1. FMARK function:

OTM3225A provided FMARK function which output signal to alert host MCU via FMARK I/O pad so that LCD display can avoid tearingr effect. FMARK output position and interval can be set by FMP[8:0] and FMI[2:0], respectively.

Figure 9-1 illustrated the FMARK output position when FMP[8:0]=9'h008.

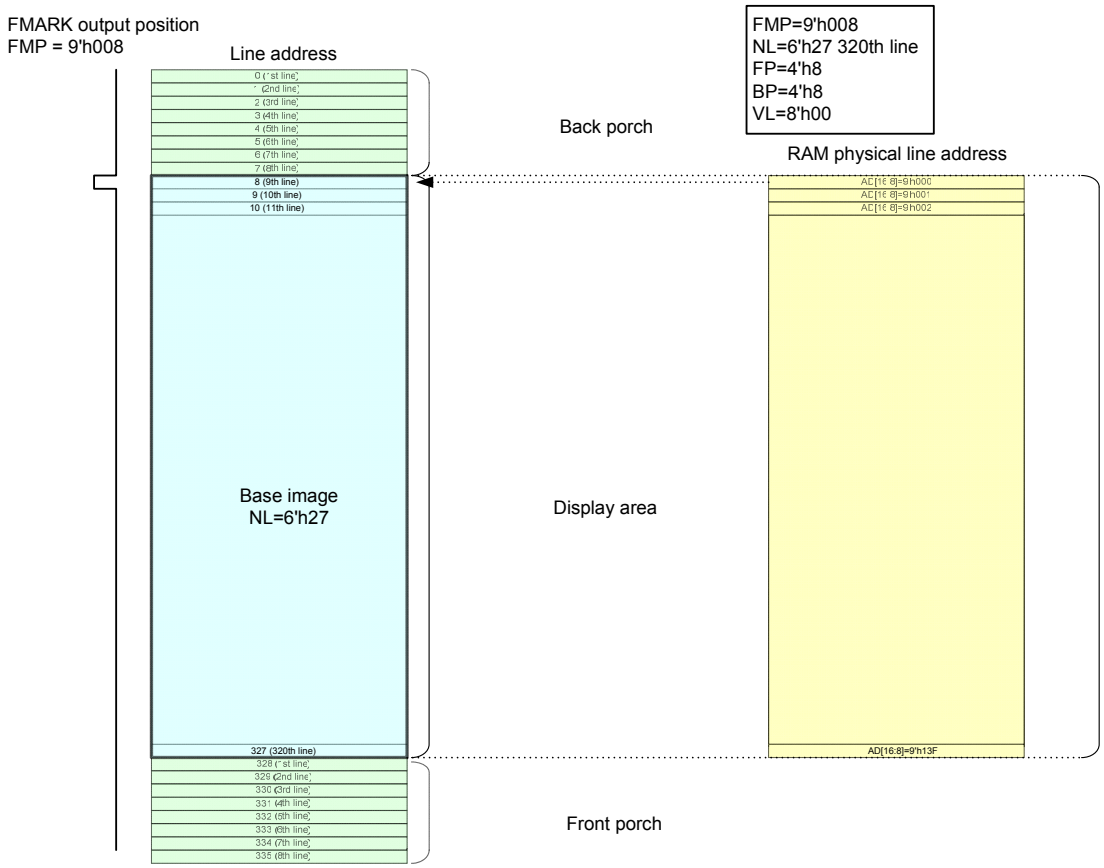
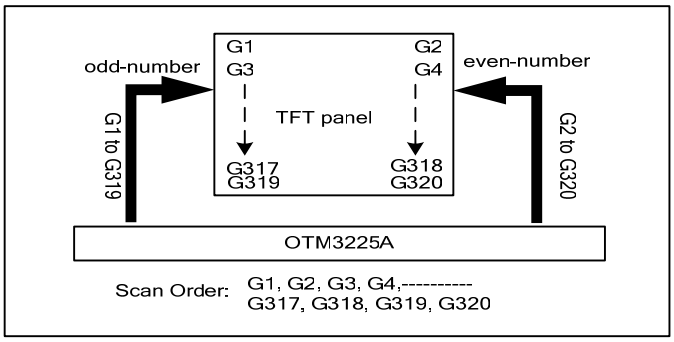
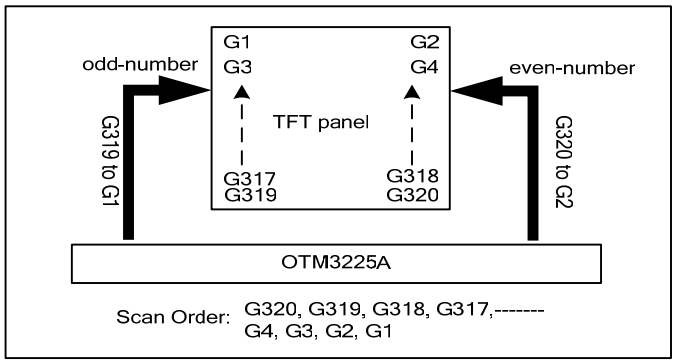
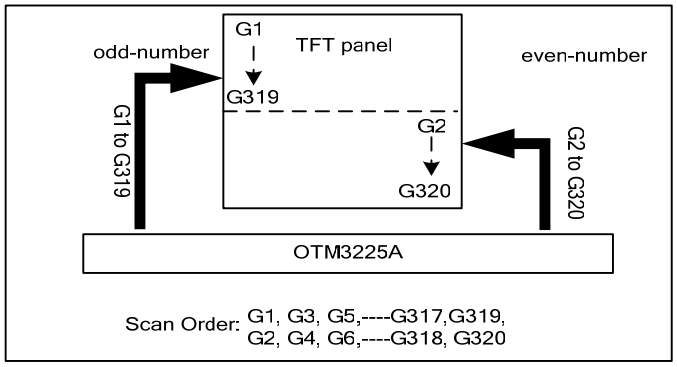
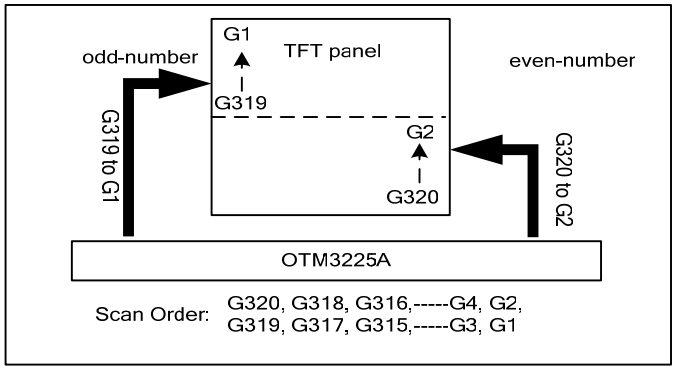


Figure 9-1 Example of FMARK signal.

9.2. Scan Mode function:

SM	GS	Scan Direction
0	0	
0	1	
1	0	
1	1	

9.3. Scaling function:

OTM3225A provides scaling function to resize the display area. The Scaling factor can be set via RSZ[1:0] (register R04h, CB [1:0]). Table summarized the RSZ[1:0] function. The image after scaling can be displayed at the area set by (HSA, HEA, VSA, VFA).

Table 9-1

RSZ[1:0]	Scaling Factor	Actual resolution (original input data 240xRGbx320)
00	No scaling	240xRGBx320
01	1/2 scaling	120xRGBx160
10	No scaling	240xRGBx320
11	1/4 scaling	60xRGBx80

Table 9-2 illustrated the data arrangement when scaling factor is 1/2, RSZ[1:0]=”01”

	1	2	3	4	5	6	7	8
1	A1	A2	A3	A4	A5	A6	A7	A8
2	B1	B2	B3	B4	B5	B6	B7	B8
3	C1	C2	C3	C4	C5	C6	C7	C8
4	D1	D2	D3	D4	D5	D6	D7	D8
5	E1	E2	E3	E4	E5	E6	E7	E8
6	F1	F2	F3	F4	F5	F6	F7	F8
7	G1	G2	G3	G4	G5	G6	G7	G8
8	H1	H1	H3	H4	H5	H6	H7	H8

	1	2	3	4
1	A1	A3	A5	A7
2	C1	C3	C5	C7
3	E1	E3	E5	E7
4	G1	G3	G5	G7

Table 9-3 data arrangement

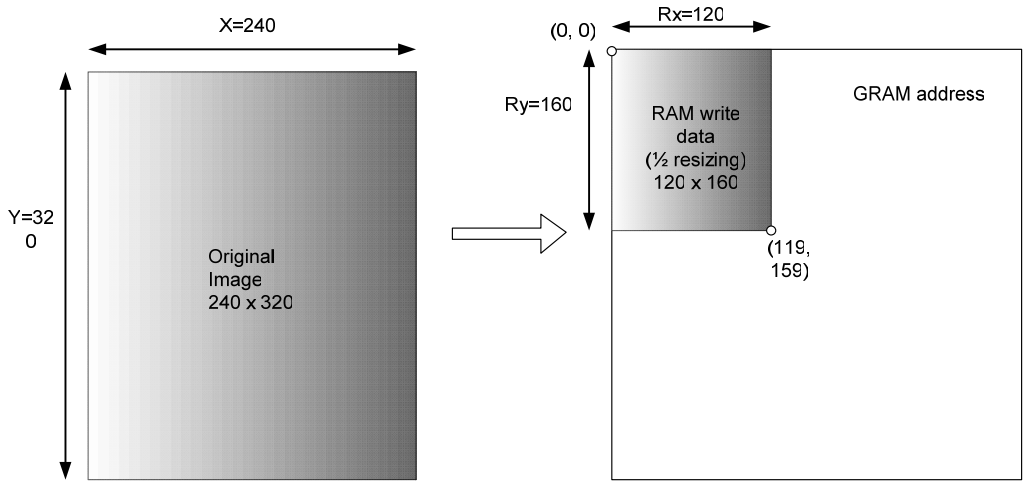
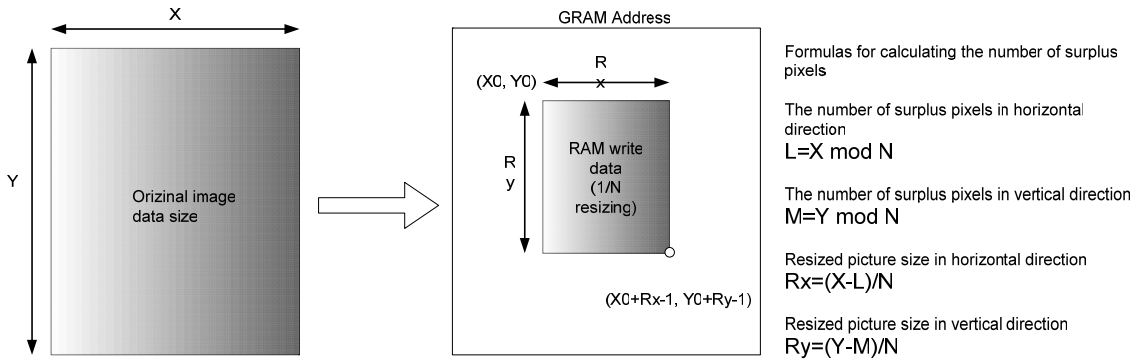
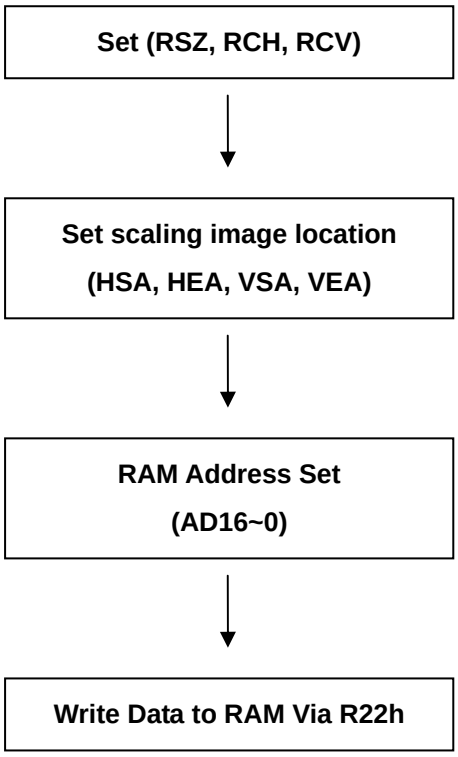


Figure 9-2 illustrated the example when scaling factor is 1/2, RSZ[1:0]=”01”



The flow chart to use scaling function:



9.4. Partial Display function:

OTM3225A has partial display function feature which can provide only partial display for power saving purpose. Partial display function can be accessed by setting BSEE=”0”,. Moreover, 2 partial display area (partial image 1/ partial image 2) can be initialized by set PTDE0=”1” and PTDE1=”1”, respectively. The partial display area for partial image 1 and partial 2 can be set by PTSA0 / PTEA0 and PTSA1/ PTEA1, respectively. **Table 9-4** and **Figure 9-3** summarized the full and partial display function.

Table 9-4 Partial display function summary table

Case	Function Setting	Display area setting	Display Position
Full display	**BASEE=”1”** **PTDE0=”x”** **PTDE1=”x”**	**(BSA,BEA)**	**-**
Partial image1:0n **Partial image2:Off**	**BASEE=”0”** **PTDE0=”1”** **PTDE1=”0”**	**(PTSA0,PTEA0)**	**PTDP0**
Partial image1:Off **Partial image2:On**	**BASEE=”0”** **PTDE0=”0”** **PTDE1=”1”**	**(PTSA1,PTEA1)**	**PTDP1**
Partail image1:On **Partial image2:On**	**BASEE=”0”** **PTDE0=”1”** **PTDE1=”1”**	**(PTSA0,PTEA0)** **(PTSA1,PTEA1)**	**PTDP0 & PTDP1**

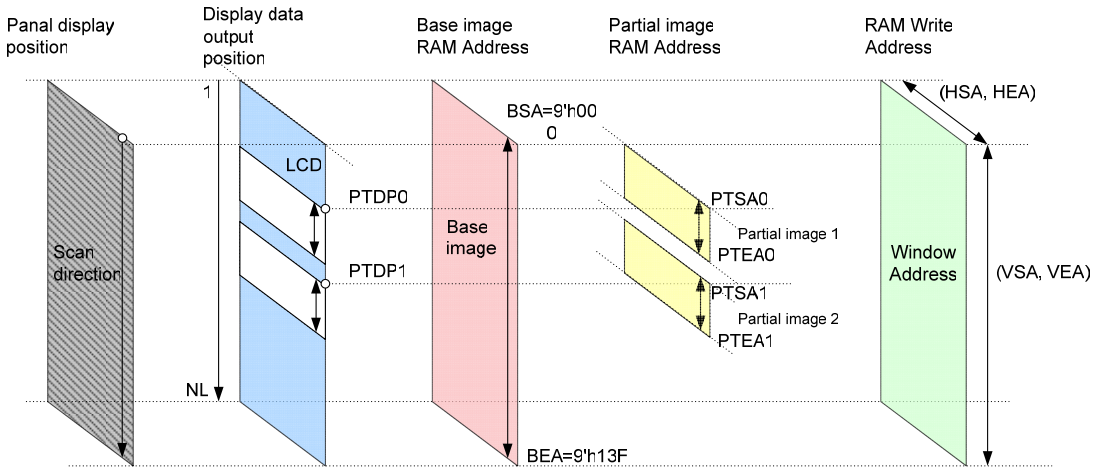


Figure 9-3 Partial display function diagram

Figure 9-4 indicated the case of NL[5:0] setting is < 6’h27 which active line is less than 320. Partial display image data can stored in not active area.

Figure 9-5 indicated the partial display area start position. The partial display area and start position can be set by (**PTSA0, PTEA0, PTSA1, PTEA1) and (PTDP0, PTDP1), respectively.**

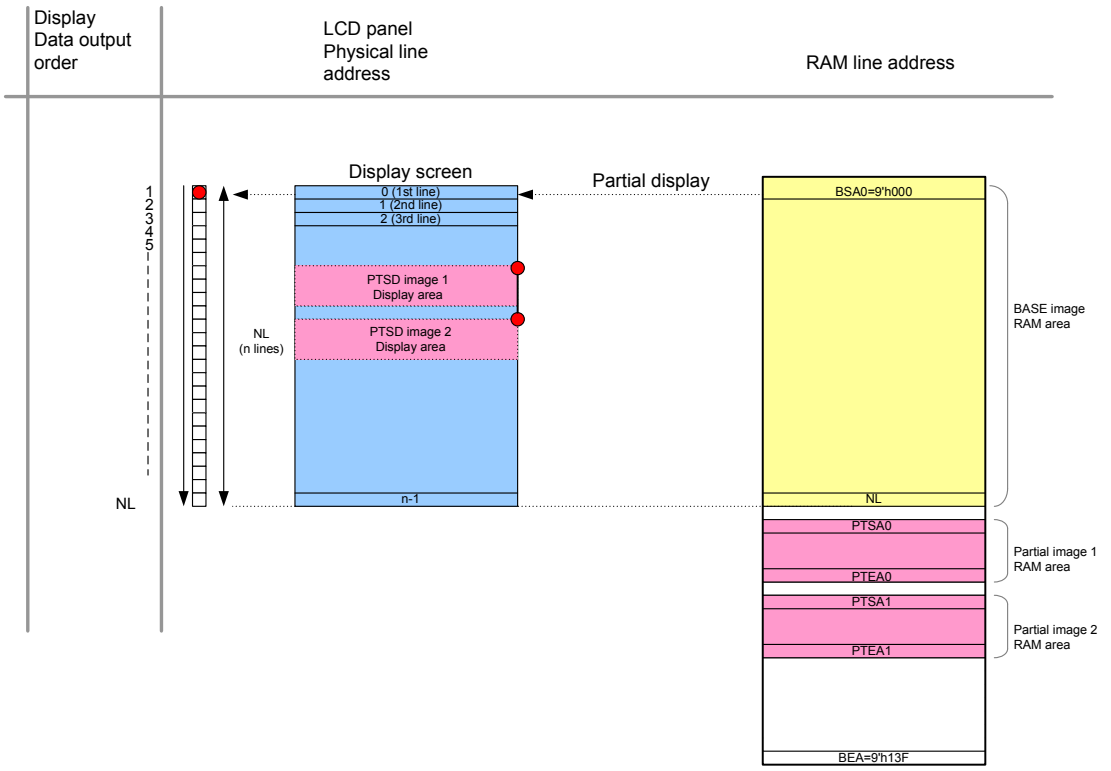


Figure 9-4 Example of NL[5:0] setting is < 6'h27 case

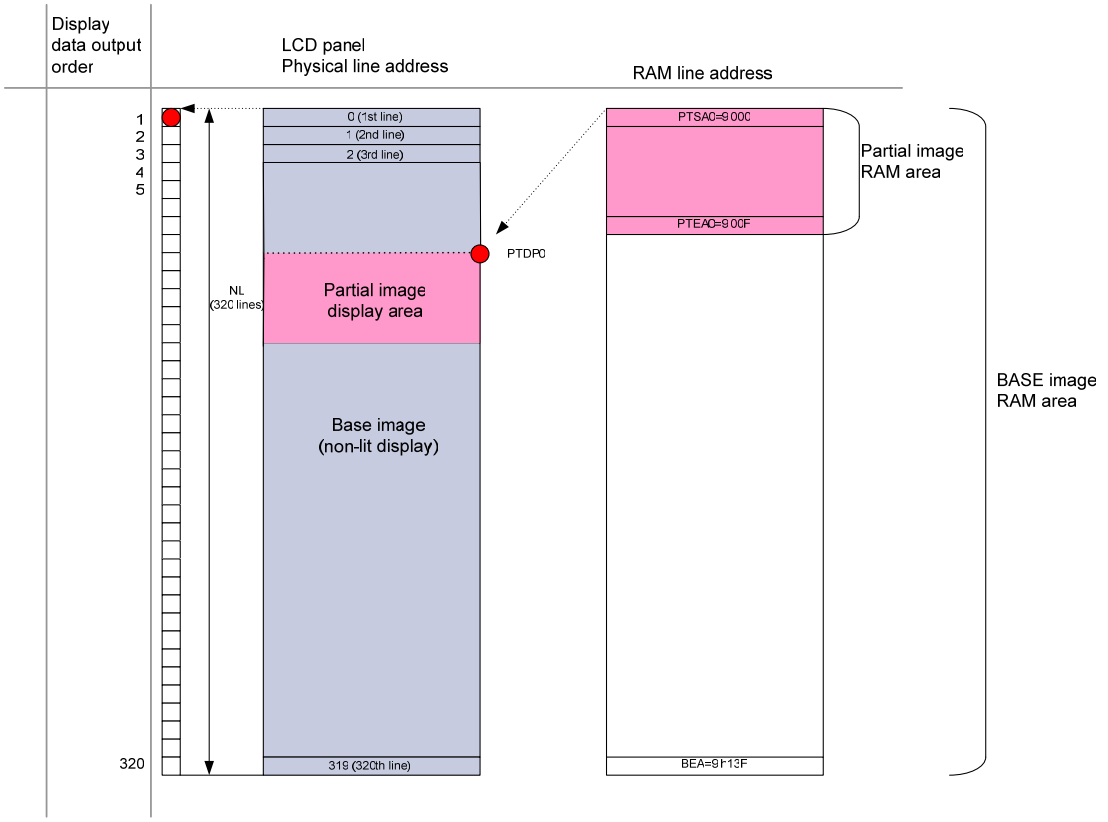


Figure 9-5 indicated the partial display area start position.

9.5. Gamma Correction functions:

	R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R30	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
R31	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
R32	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
R35	W	1	0	0	0	0	0	RP1[2]	RP1[2]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[2]	RP0[0]
R36	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R37	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
R38	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
R39	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
R3C	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
R3D	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

γ **Control (R30h to R3Dh):** OTM3225A provides 10 gamma registers to fine tune gamma output voltage.

KP5-0[2:0]: γ **fine tune** registers for positive polarity.

RP1-0[2:0]: γ **gradient** registers for positive polarity.

VRP1-0[4:0]: γ **amplitude** registers for positive polarity.

KN5-0[2:0]: γ **fine tune** registers for positive polarity.

RN1-0[2:0]: γ **gradient** registers for positive polarity.

VRN1-0[4:0]: γ **amplitude** registers for positive polarity.

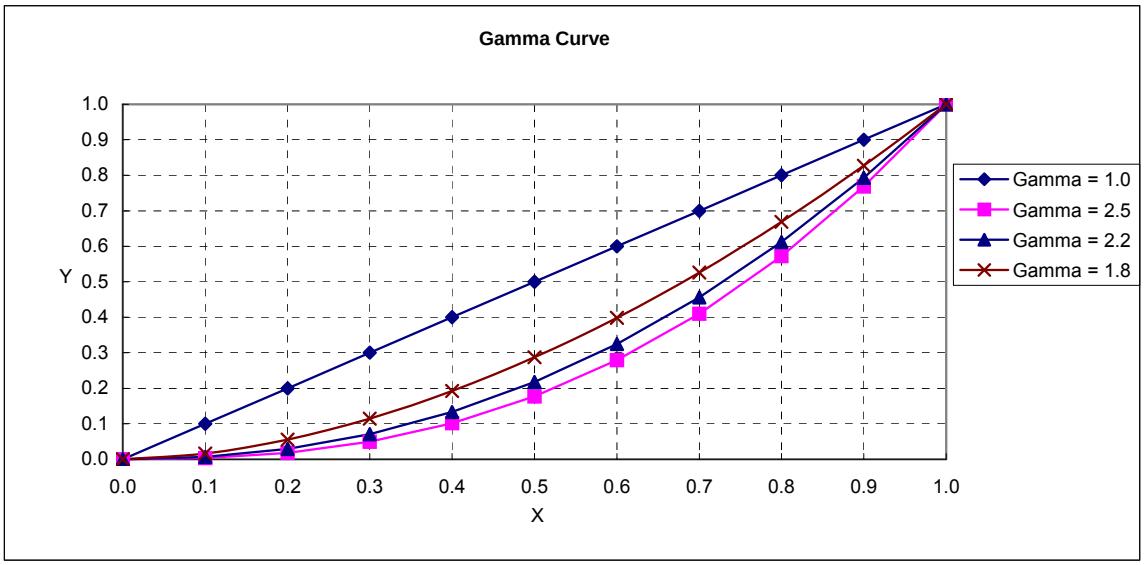
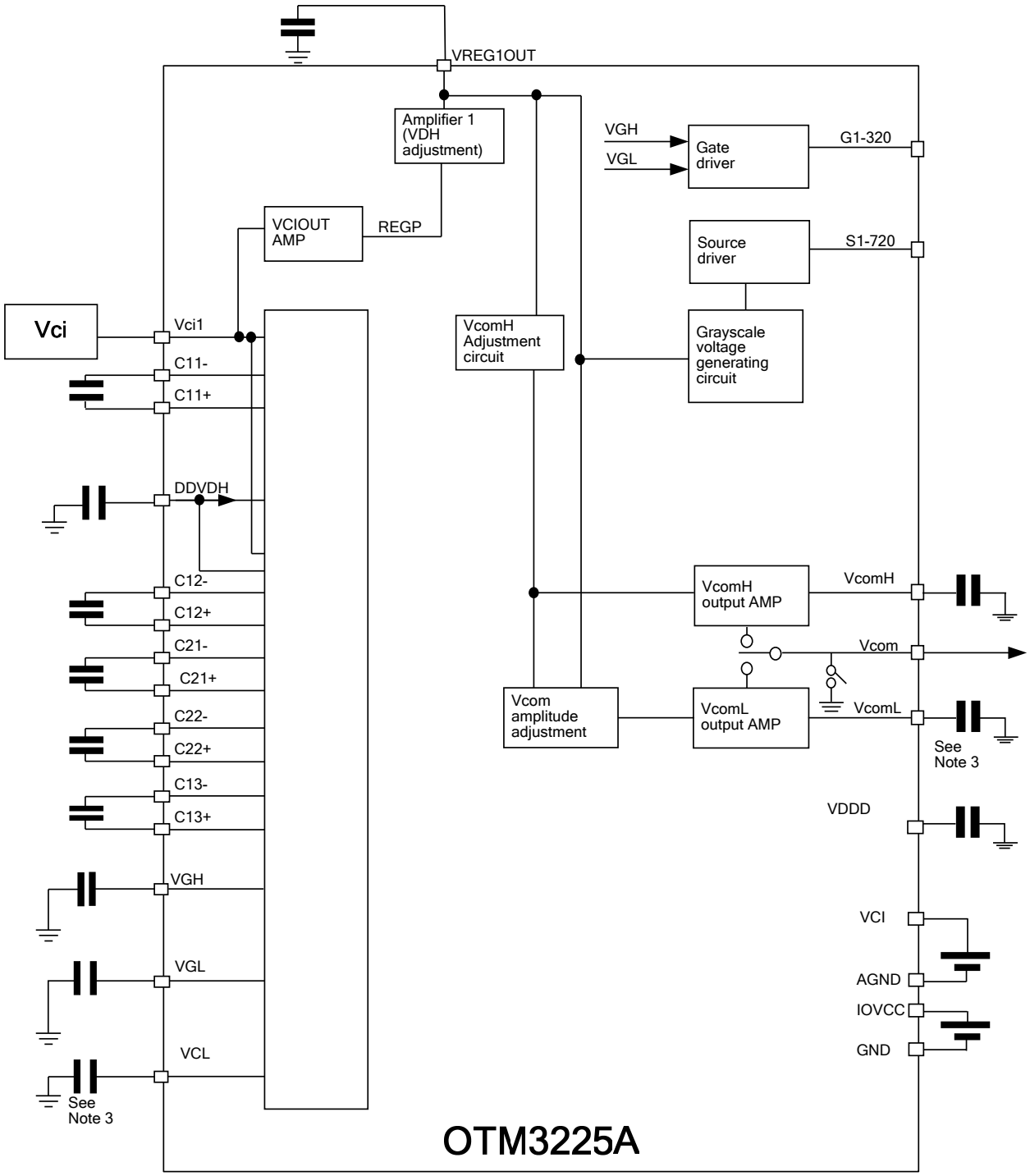


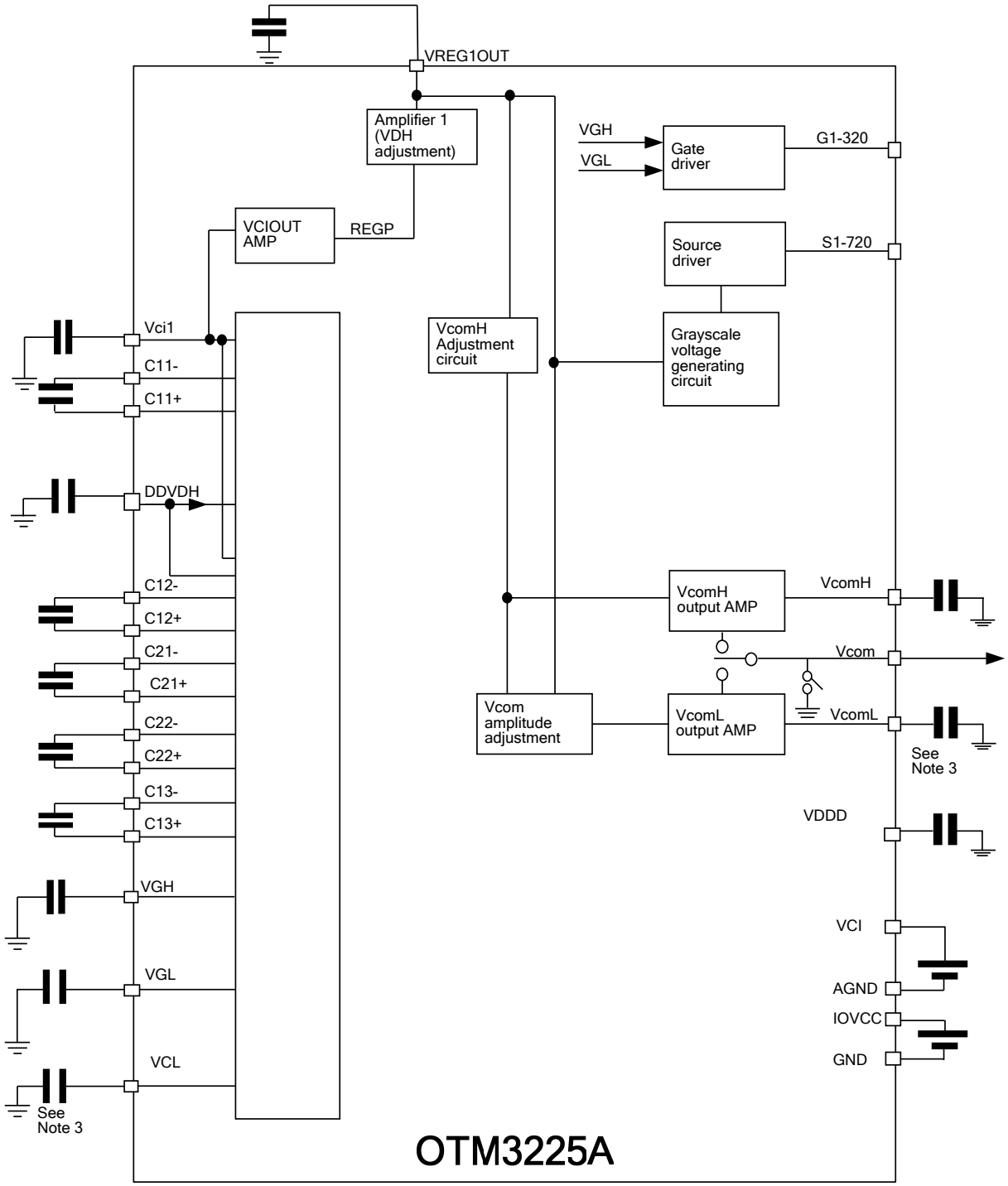
Figure 9-6 Illustrated 4 different Gamma Curve.

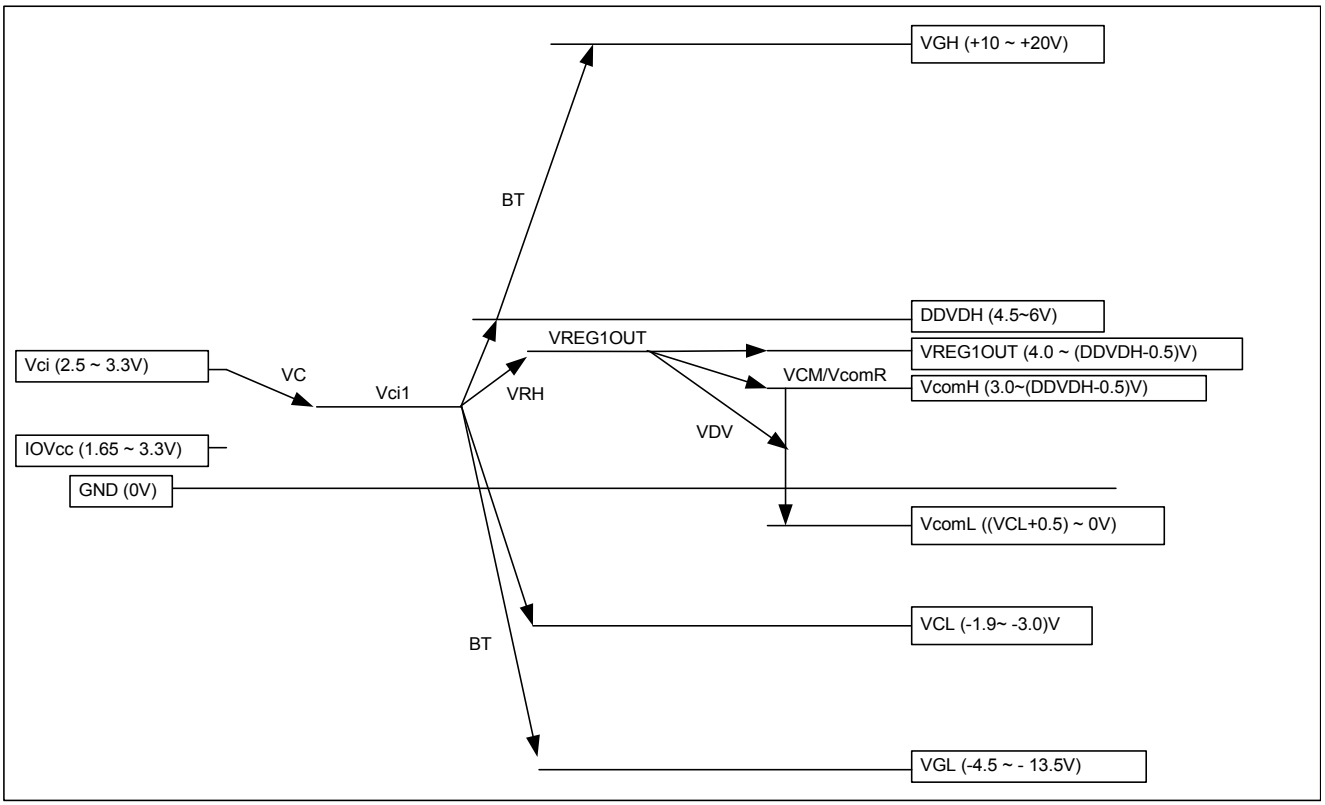
10. Power Management System:

(a) VCI short VCI1:

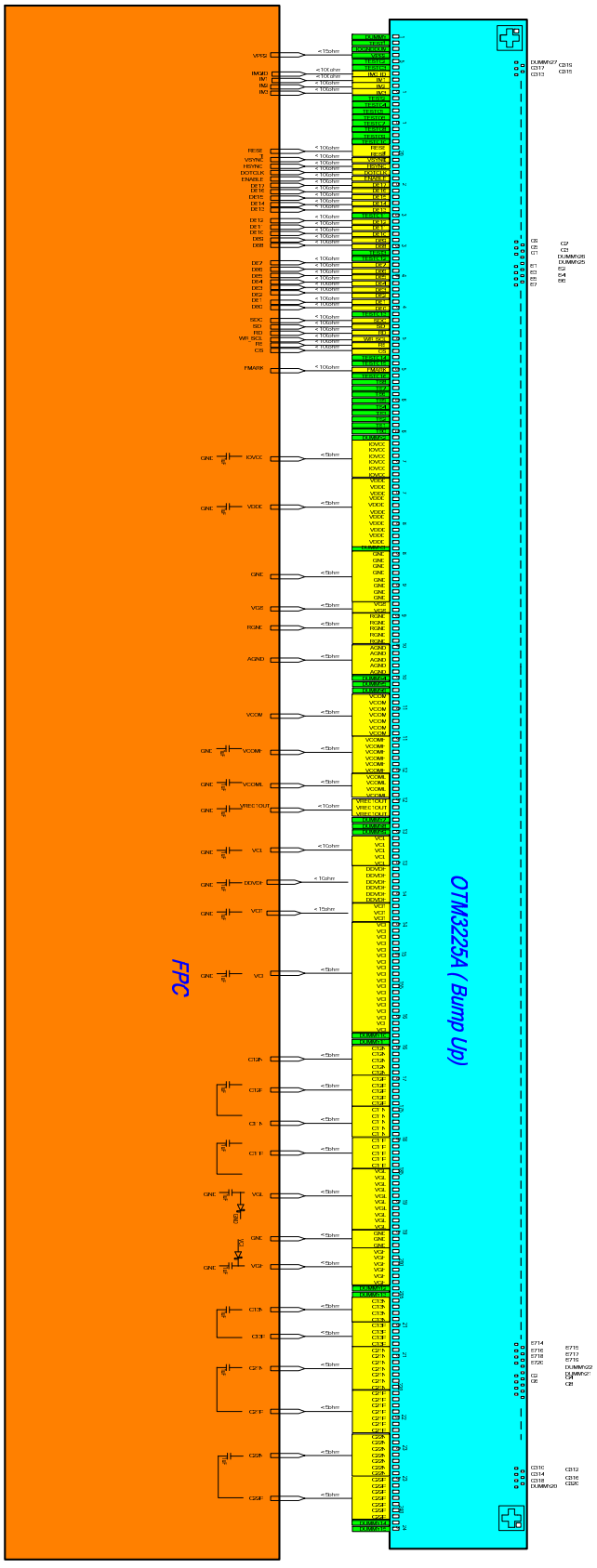


(b) Separate VCI and VCI1:




VGH (+10 ~ +20V)
BT
DDVDH (4.5~6V)
VREG1OUT
VREG1OUT (4.0 ~ (DDVDH-0.5)V)
Vci (2.5 ~ 3.3V)
VC
Vci1
VRH
VCM/VcomR
VcomH (3.0~(DDVDH-0.5)V)
VDV
IOVcc (1.65 ~ 3.3V)
GND (0V)
VcomL ((VCL+0.5) ~ 0V)
VCL (-1.9~ -3.0)V
BT
VGL (-4.5 ~ - 13.5V)

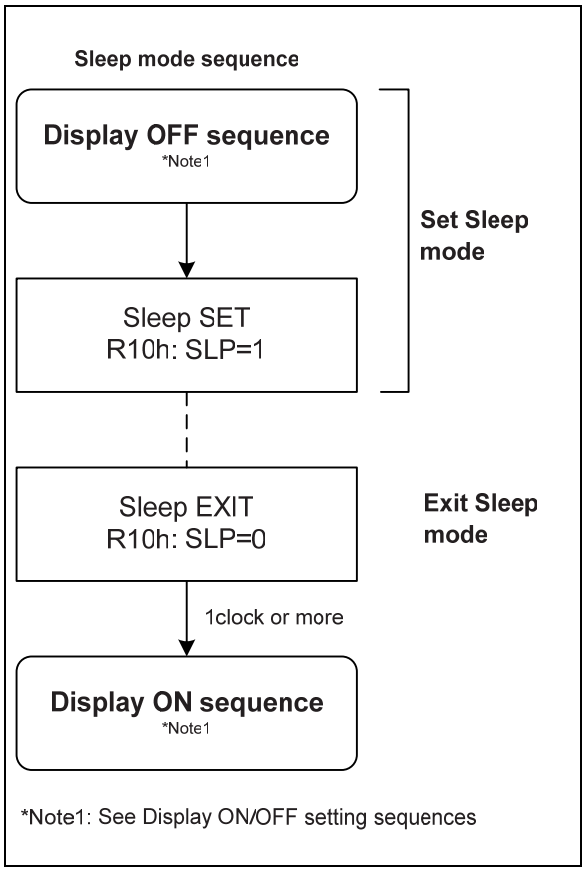
11. Application circuits:



12. Initial Code:

This initial code is not including Gamma setting. Please contact Orise Technology for desired Gamma setting.

12.1. Sequence to exit sleep mode:



13. Electrical Characteristics:

13.1. Absolute Maximum Ratings:

Table 13-1

Item	Symbol	Unit	Value	Note
Power Supply Voltage1	IOVCC – GND	V	-0.3 ～+4.6	
Power Supply Voltage 2	VCI – AGND	V	-0.3 ～+4.6	
Power Supply Voltage 3	DDVDH – AGND	V	-0.3 ～+6.5	
Power Supply Voltage4	AGND – VCL	V	-0.3 ～+4.6	
Power Supply Voltage 5	DDVDH – VCL	V	-0.3 ～+9.0	
Power Supply Voltage7	AGND – VGL	V	-0.3 ～+14.0	
Power Supply Voltage 8	VGH– VGL	V	-0.3 ～+30.0	
Input Voltage	Vt	V	-0.3 ～IOVCC + 0.3	
Operating Temperature	Topr	℃	-40 ～+85	
Storage Temperature	Tstg	℃	-55 ～+110	

13.2. DC Characteristics

Table 13-2 VCI= 2.50V～3.30V, IOVCC=1.65V～ 3.30V, Ta=-40℃～+85℃

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input High level voltage	VIH	V	IOVCC=1.65V～3.30V	0.8xIOVCC	-	IOVCC	
Input Low level voltage	VIL	V	IOVCC=1.65V～3.30V	-0.3	-	0.2xIOVCC	
Output ”High” level voltage 1 (DB0-17)	VOH	V	IOVCC=1.65V～3.30V, IOH=-0.1mA	0.8xIOVCC	-	-	
Output ”Low” level voltage 1 (DB0-17)	VOL	V	IOVCC=1.65V～3.30V, IOL=0.1mA	-	-	0.2xIOVCC	
I/O leak current	ILI	μA	Vin=0～IOVCC	-1	-	1	

13.3. AC Characteristics

VCI= 2.50V～3.30V，IOVCC=1.65V～3.30V，Ta=-40℃～+85℃

13.3.1. Clock Characteristics

Table 13-3

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.	Note
RC Oscillation clock	fosc	kHz	IOVCC = VCI = 3.0V, 25°C		TBD		9

13.3.2. 80-System Bus Interface Timing Characteristics (18-/ 16- bit interface)

Table 13-4 Normal write operation, IOVCC=1.65V~3.30V

Item	Symbol		Unit	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	125	-	-
	Read	tCYCR	ns	450	-	-
Write low-level pulse width		PWLW	ns	45	-	-
Read low-level pulse width		PWLR	ns	170	-	-
Write high-level pulse width		PWHW	ns	70	-	-
Read high-level pulse width		PWHR	ns	250	-	-
Write/Read rise/ fall time		tWRr, WRf	ns	-	-	25
Setup time	Write (RS to CS*,WR*)	tAS	ns	0	-	-
	Read (RS to CS*, RD*)		ns	10	-	-
Address Hold Time		tAH	ns	2	-	-
Write data setup time		tDSW	ns	25	-	-
Write data hold time		tH	ns	10	-	-
Read data delay time		tDDR	ns	-	-	150
Read data hold time		tDHR	ns	5	-	-

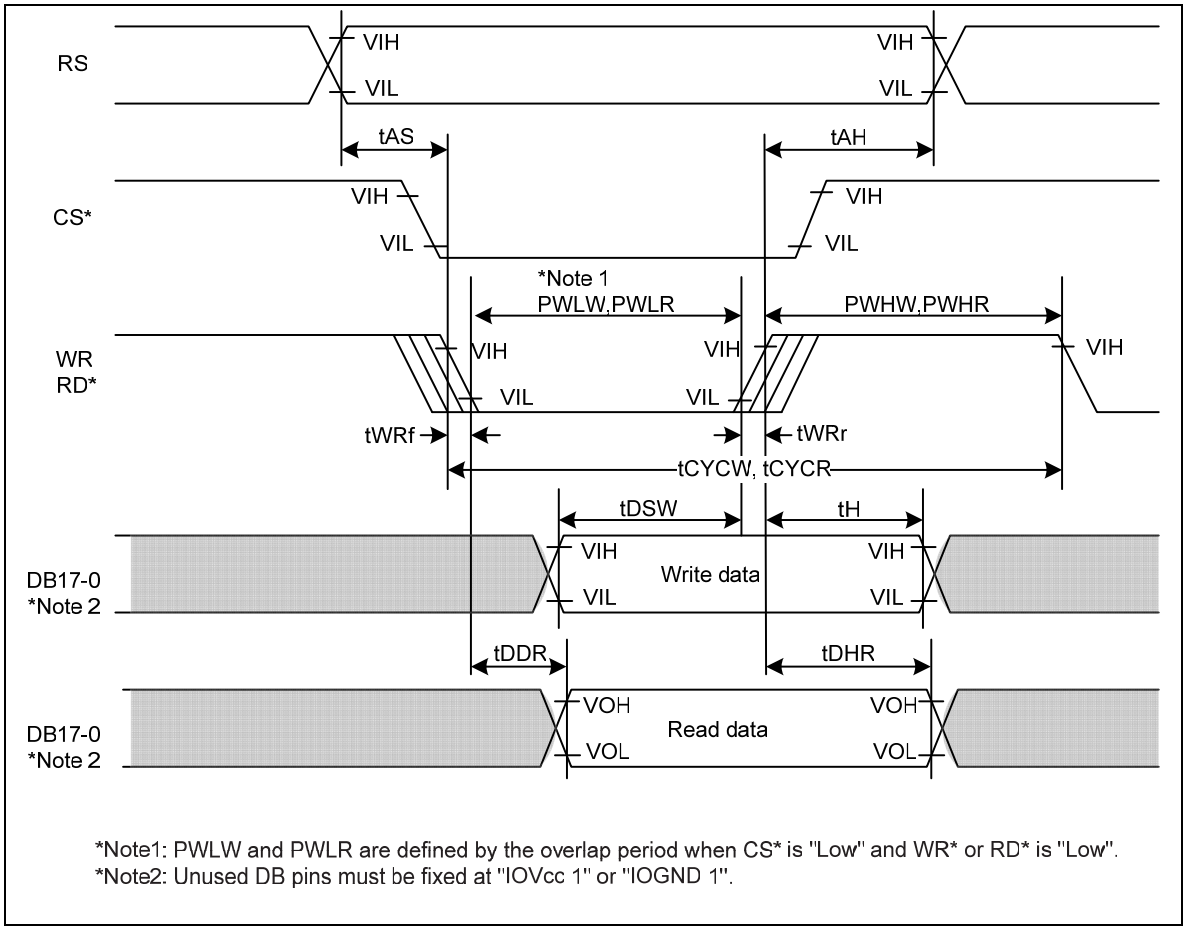


Figure 13-1 80-System Bus Interface

13.3.3. Clock-synchronized Serial Interface Timing Characteristics

Normal Write Function(IOVCC=1.65~3.30V)

Table 13-5

Item	Symbol		Unit	Min.	Typ.	Max.
Serial Time Clock Cycle	Write (received)	tSCYC	ns	100	-	20.000
	Read (transmitted)	tSCYC	ns	350	-	20.000
Serial Clock high-level width	Write (received)	tSCH	ns	40	-	-
	Read (transmitted)	tSCH	ns	150	-	-
Serial Clock low-level width	Write (received)	tSCL	ns	40	-	-
	Read (transmitted)	tSCL	ns	150	-	-
Serial clock rise/fall time		tSCr, tSCf	ns	-	-	20
Chip select setup time		tCSU	ns	20	-	-
Chip select hold time		tCH	ns	60	-	-
Serial input data setup time		tSISU	ns	30	-	-
Serial input data hold time		tSIH	ns	30	-	-
Serial output data delay time		tSOD	ns	-	-	130
Serial output data hold time		tSOH	ns	5	-	-

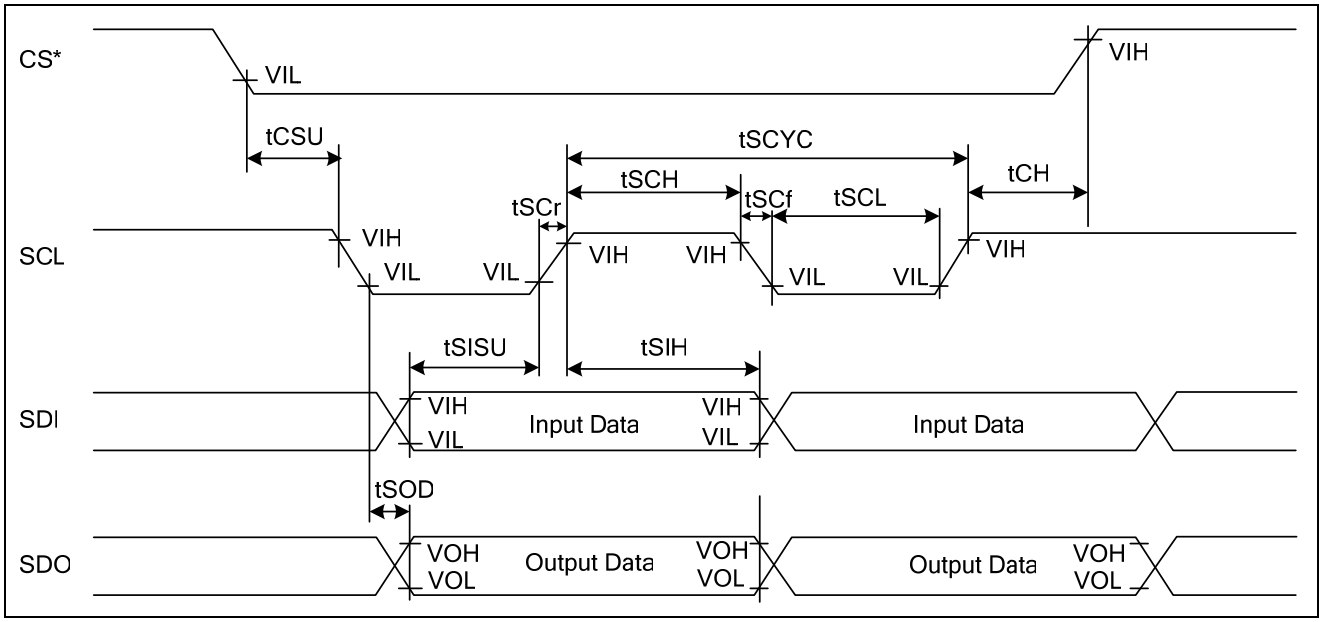


Figure 13-2 SPI interface Timing Diagram

13.3.4. Reset Timing Characteristics (IOVCC=1.65~3.30V)

Table 13-6

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	tRES	ms	1	–	–
Reset rise time	trRES	μs	–	–	10

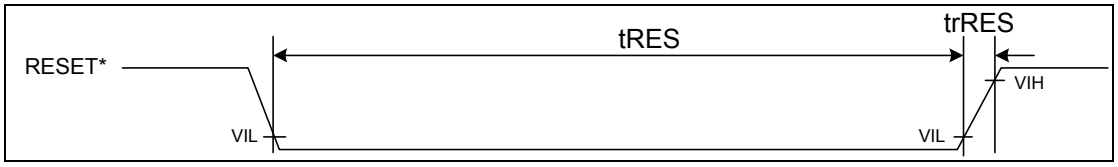


Figure 13-3 Reset Operation

13.3.5. RGB Interface Timing Characteristics

18-/ 16- bit RGB interface, IOVCC=1.65~3.30V

Table 13-7

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC Setup time	tSYNCS	clock	0	-	1
ENABLE Setup time	tENS	ns	10	-	-
ENABLE Hold time	tENH	ns	20	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-
DOTCLK cycle time	tCYCD	ns	100	-	-
Data setup time	tPDS	ns	10	-	-
Data hold time	tPDH	ns	40	-	-
DOTCLK, VSYNC and HSYNC rise/fall time	trgbr trgbf	ns	-	-	25

6-bit RGB interface, IOVCC=1.65~3.30V

Table 13-8

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	clock	0	-	1
ENABLE setup time	tENS	ns	10	-	-
ENABLE hold time	tENH	ns	25	-	-
DOTCLK low-level pulse width	PWDL	ns	25	-	-
DOTCLK high-level pulse width	PWDH	ns	25	-	-
DOTCLK cycle time	tCYCD	ns	60	-	-
Data setup-time	tPDS	ns	10	-	-
Data hold time	tPDH	ns	25	-	-
DOTCLK, VSYNC, and HSYNC rise/fall time	trgb ttrgbf	ns	-	-	25

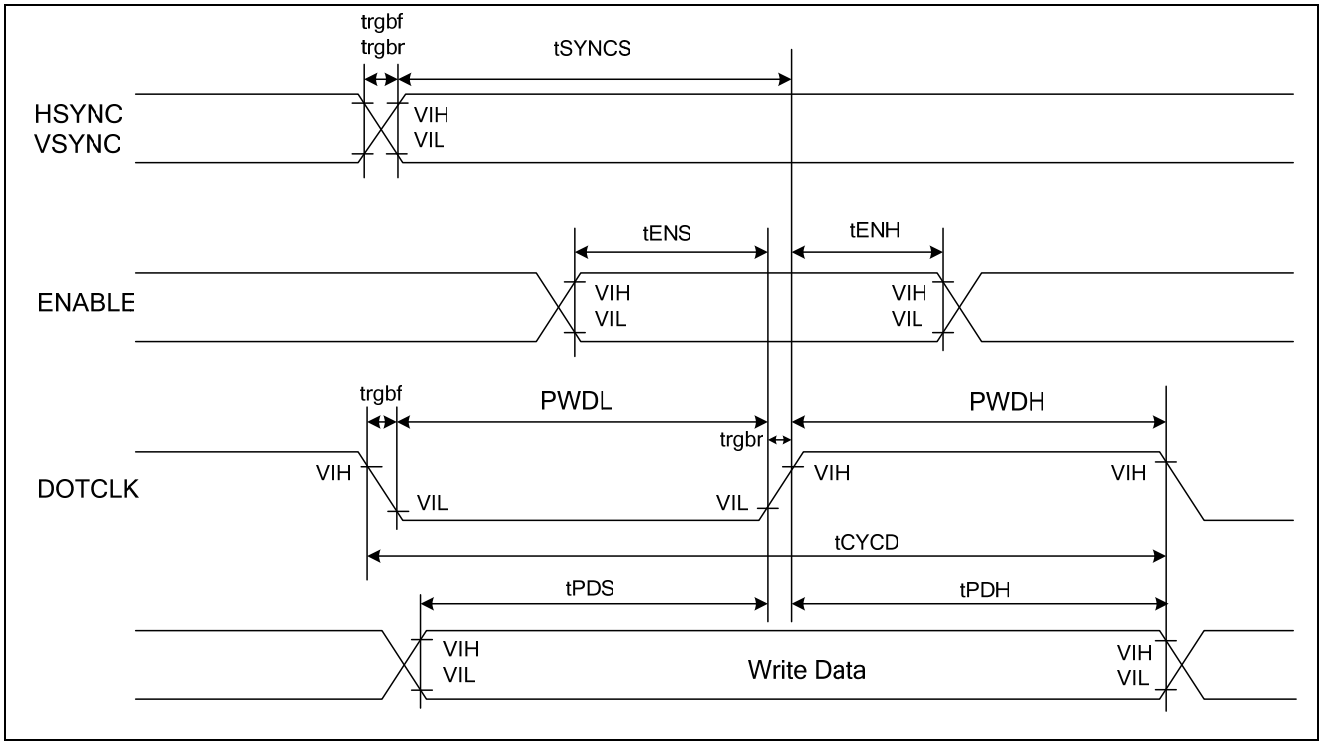


Figure 13-4 RGB interface AC timing Diagram

14. CHIP INFORMATION

14.1. PAD Assignment

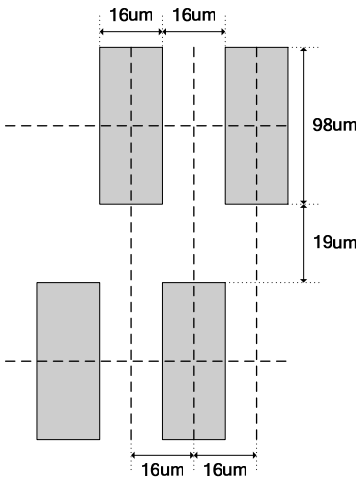
OTM3225A (Bump Up)

14.2. PAD Dimension

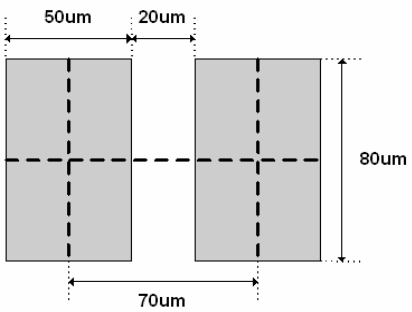
Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	17820	865	μm
Chip thickness	-	400 ± 20		
Pad pitch	1~243	70	-	
	244~1291	16	-	
Pad size	1~243	50	80	
	244~1291	16	98	

Note1: Chip size included scribe line.

14.2.1. Output Pads



14.2.2. Input Pads



14.3. Bump Characteristics

Item	Standard	Note
Bump Hardness	75Hv	± 25Hv
Bump Height	15μm	± 3μm
Co-planarity (in Chip)	R≦ 2μm	R : Max-Min
Roughness (in Bump)	R≦ 2μm	R : Max-Min
Bump Size	Long side ± 2.5μm, short side ± 2.5μm Long side ± 2.5μm, short side ± 2μm	bump pitch＞20μm bump pitch≦20μm
Shear Force	> 5 g/mil^2	

14.4. PAD Locations

No.	Pad Name	X	Y
1	DUMMY1	-8610	-307.5
2	TEST1	-8540	-307.5
3	IOGNDDUM	-8470	-307.5
4	VPP2	-8400	-307.5
5	TESTO2	-8330	-307.5
6	TESTO3	-8260	-307.5
7	IM0_ID	-8190	-307.5
8	IM1	-8120	-307.5
9	IM2	-8050	-307.5
10	IM3	-7980	-307.5
11	TEST2	-7910	-307.5
12	TESTO4	-7840	-307.5
13	TESTO5	-7770	-307.5
14	TESTO6	-7700	-307.5
15	TESTO7	-7630	-307.5
16	TESTO8	-7560	-307.5
17	TESTO9	-7490	-307.5
18	TESTO10	-7420	-307.5
19	RESET	-7350	-307.5
20	RESET	-7280	-307.5
21	VSYNC	-7210	-307.5
22	HSYNC	-7140	-307.5
23	DOTCLK	-7070	-307.5
24	ENABLE	-7000	-307.5
25	DB17	-6905	-307.5
26	DB16	-6825	-307.5
27	DB15	-6745	-307.5
28	DB14	-6665	-307.5
29	DB13	-6585	-307.5
30	TESTO11	-6495	-307.5
31	DB12	-6405	-307.5
32	DB11	-6325	-307.5
33	DB10	-6245	-307.5
34	DB9	-6165	-307.5
35	DB8	-6085	-307.5
36	TEST3	-5990	-307.5
37	TESTO12	-5920	-307.5
38	DB7	-5825	-307.5
39	DB6	-5745	-307.5
40	DB5	-5665	-307.5
41	DB4	-5585	-307.5
42	DB3	-5505	-307.5
43	DB2	-5425	-307.5
44	DB1	-5345	-307.5
45	DB0	-5265	-307.5
46	TESTO13	-5180	-307.5
47	SDO	-5110	-307.5
48	SDI	-5040	-307.5
49	RD	-4970	-307.5
50	WR_SCL	-4900	-307.5
51	RS	-4830	-307.5
52	CS	-4760	-307.5
53	TESTO14	-4690	-307.5
54	TESTO15	-4620	-307.5
55	FMARK	-4550	-307.5
56	TESTO16	-4480	-307.5
57	TS8	-4410	-307.5
58	TS7	-4340	-307.5
59	TS6	-4270	-307.5
60	TS5	-4200	-307.5
61	TS4	-4130	-307.5
62	TS3	-4060	-307.5
63	TS2	-3990	-307.5
64	TS1	-3920	-307.5
65	TS0	-3850	-307.5
66	DUMMY2	-3780	-307.5
67	IOVCC	-3710	-307.5
68	IOVCC	-3640	-307.5
69	IOVCC	-3570	-307.5
70	IOVCC	-3500	-307.5
71	IOVCC	-3430	-307.5
72	IOVCC	-3360	-307.5
73	VDDD	-3290	-307.5
74	VDDD	-3220	-307.5
75	VDDD	-3150	-307.5
76	VDDD	-3080	-307.5
77	VDDD	-3010	-307.5
78	VDDD	-2940	-307.5
79	VDDD	-2870	-307.5
80	VDDD	-2800	-307.5
81	VDDD	-2730	-307.5
82	VDDD	-2660	-307.5
83	VDDD	-2590	-307.5
84	DUMMY3	-2520	-307.5
85	GND	-2450	-307.5
86	GND	-2380	-307.5
87	GND	-2310	-307.5
88	GND	-2240	-307.5
89	GND	-2170	-307.5
90	GND	-2100	-307.5
91	GND	-2030	-307.5
92	GND	-1960	-307.5
93	VGS	-1890	-307.5
94	VGS	-1820	-307.5
95	RGND	-1750	-307.5
96	RGND	-1680	-307.5
97	RGND	-1610	-307.5
98	RGND	-1540	-307.5
99	RGND	-1470	-307.5
100	AGND	-1400	-307.5
101	AGND	-1330	-307.5
102	AGND	-1260	-307.5
103	AGND	-1190	-307.5
104	AGND	-1120	-307.5
105	DUMMY4	-1050	-307.5
106	DUMMY5	-980	-307.5
107	DUMMY6	-910	-307.5
108	VCOM	-840	-307.5
109	VCOM	-770	-307.5
110	VCOM	-700	-307.5
111	VCOM	-630	-307.5

No.	Pad Name	X	Y
112	VCOM	-560	-307.5
113	VCOM	-490	-307.5
114	VCOM	-420	-307.5
115	VCOMH	-350	-307.5
116	VCOMH	-280	-307.5
117	VCOMH	-210	-307.5
118	VCOMH	-140	-307.5
119	VCOMH	-70	-307.5
120	VCOMH	0	-307.5
121	VCOML	70	-307.5
122	VCOML	140	-307.5
123	VCOML	210	-307.5
124	VCOML	280	-307.5
125	VREG1OUT	350	-307.5
126	VREG1OUT	420	-307.5
127	VREG1OUT	490	-307.5
128	DUMMY7	560	-307.5
129	DUMMY8	630	-307.5
130	DUMMY9	700	-307.5
131	VCL	770	-307.5
132	VCL	840	-307.5
133	VCL	910	-307.5
134	VCL	980	-307.5
135	VCL	1050	-307.5
136	DDVDH	1120	-307.5
137	DDVDH	1190	-307.5
138	DDVDH	1260	-307.5
139	DDVDH	1330	-307.5
140	DDVDH	1400	-307.5
141	DDVDH	1470	-307.5
142	VCI1	1540	-307.5
143	VCI1	1610	-307.5
144	VCI1	1680	-307.5
145	VCI	1750	-307.5
146	VCI	1820	-307.5
147	VCI	1890	-307.5
148	VCI	1960	-307.5
149	VCI	2030	-307.5
150	VCI	2100	-307.5
151	VCI	2170	-307.5
152	VCI	2240	-307.5
153	VCI	2310	-307.5
154	VCI	2380	-307.5
155	VCI	2450	-307.5
156	VCI	2520	-307.5
157	VCI	2590	-307.5
158	VCI	2660	-307.5
159	VCI	2730	-307.5
160	VCI	2800	-307.5
161	VCI	2870	-307.5
162	VCI	2940	-307.5
163	DUMMY10	3010	-307.5
164	DUMMY11	3080	-307.5
165	C12N	3150	-307.5
166	C12N	3220	-307.5
167	C12N	3290	-307.5
168	C12N	3360	-307.5
169	C12N	3430	-307.5
170	C12P	3500	-307.5
171	C12P	3570	-307.5
172	C12P	3640	-307.5
173	C12P	3710	-307.5
174	C12P	3780	-307.5
175	C11N	3850	-307.5
176	C11N	3920	-307.5
177	C11N	3990	-307.5
178	C11N	4060	-307.5
179	C11N	4130	-307.5
180	C11P	4200	-307.5
181	C11P	4270	-307.5
182	C11P	4340	-307.5
183	C11P	4410	-307.5
184	C11P	4480	-307.5
185	VGL	4550	-307.5
186	VGL	4620	-307.5
187	VGL	4690	-307.5
188	VGL	4760	-307.5
189	VGL	4830	-307.5
190	VGL	4900	-307.5
191	VGL	4970	-307.5
192	VGL	5040	-307.5
193	VGL	5110	-307.5
194	VGL	5180	-307.5
195	GND	5250	-307.5
196	GND	5320	-307.5
197	GND	5390	-307.5
198	VGH	5460	-307.5
199	VGH	5530	-307.5
200	VGH	5600	-307.5
201	VGH	5670	-307.5
202	VGH	5740	-307.5
203	VGH	5810	-307.5
204	DUMMY12	5880	-307.5
205	DUMMY13	5950	-307.5
206	C13N	6020	-307.5
207	C13N	6090	-307.5
208	C13N	6160	-307.5
209	C13N	6230	-307.5
210	C13P	6300	-307.5
211	C13P	6370	-307.5
212	C13P	6440	-307.5
213	C13P	6510	-307.5
214	C21N	6580	-307.5
215	C21N	6650	-307.5
216	C21N	6720	-307.5
217	C21N	6790	-307.5
218	C21N	6860	-307.5
219	C21N	6930	-307.5
220	C21N	7000	-307.5
221	C21P	7070	-307.5
222	C21P	7140	-307.5
223	C21P	7210	-307.5
224	C21P	7280	-307.5
225	C21P	7350	-307.5
226	C21P	7420	-307.5
227	C21P	7490	-307.5
228	C22N	7560	-307.5
229	C22N	7630	-307.5
230	C22N	7700	-307.5
231	C22N	7770	-307.5
232	C22N	7840	-307.5
233	C22N	7910	-307.5
234	C22N	7980	-307.5
235	C22P	8050	-307.5
236	C22P	8120	-307.5
237	C22P	8190	-307.5
238	C22P	8260	-307.5
239	C22P	8330	-307.5
240	C22P	8400	-307.5
241	C22P	8470	-307.5
242	DUMMY14	8540	-307.5
243	DUMMY15	8610	-307.5
244	DUMMY20	8659	202.5
245	G320	8643	319.5
246	G318	8627	202.5
247	G316	8611	319.5
248	G314	8595	202.5
249	G312	8579	319.5
250	G310	8563	202.5
251	G308	8547	319.5
252	G306	8531	202.5
253	G304	8515	319.5
254	G302	8499	202.5
255	G300	8483	319.5
256	G298	8467	202.5
257	G296	8451	319.5
258	G294	8435	202.5
259	G292	8419	319.5
260	G290	8403	202.5
261	G288	8387	319.5
262	G286	8371	202.5
263	G284	8355	319.5
264	G282	8339	202.5
265	G280	8323	319.5
266	G278	8307	202.5
267	G276	8291	319.5
268	G274	8275	202.5
269	G272	8259	319.5
270	G270	8243	202.5
271	G268	8227	319.5
272	G266	8211	202.5
273	G264	8195	319.5
274	G262	8179	202.5
275	G260	8163	319.5
276	G258	8147	202.5

No.	Pad Name	X	Y
277	G256	8131	319.5
278	G254	8115	202.5
279	G252	8099	319.5
280	G250	8083	202.5
281	G248	8067	319.5
282	G246	8051	202.5
283	G244	8035	319.5
284	G242	8019	202.5
285	G240	8003	319.5
286	G238	7987	202.5
287	G236	7971	319.5
288	G234	7955	202.5
289	G232	7939	319.5
290	G230	7923	202.5
291	G228	7907	319.5
292	G226	7891	202.5
293	G224	7875	319.5
294	G222	7859	202.5
295	G220	7843	319.5
296	G218	7827	202.5
297	G216	7811	319.5
298	G214	7795	202.5
299	G212	7779	319.5
300	G210	7763	202.5
301	G208	7747	319.5
302	G206	7731	202.5
303	G204	7715	319.5
304	G202	7699	202.5
305	G200	7683	319.5
306	G198	7667	202.5
307	G196	7651	319.5
308	G194	7635	202.5
309	G192	7619	319.5
310	G190	7603	202.5
311	G188	7587	319.5
312	G186	7571	202.5
313	G184	7555	319.5
314	G182	7539	202.5
315	G180	7523	319.5
316	G178	7507	202.5
317	G176	7491	319.5
318	G174	7475	202.5
319	G172	7459	319.5
320	G170	7443	202.5
321	G168	7427	319.5
322	G166	7411	202.5
323	G164	7395	319.5
324	G162	7379	202.5
325	G160	7363	319.5
326	G158	7347	202.5
327	G156	7331	319.5
328	G154	7315	202.5
329	G152	7299	319.5
330	G150	7283	202.5
331	G148	7267	319.5
332	G146	7251	202.5
333	G144	7235	319.5
334	G142	7219	202.5
335	G140	7203	319.5
336	G138	7187	202.5
337	G136	7171	319.5
338	G134	7155	202.5
339	G132	7139	319.5
340	G130	7123	202.5
341	G128	7107	319.5
342	G126	7091	202.5
343	G124	7075	319.5
344	G122	7059	202.5
345	G120	7043	319.5
346	G118	7027	202.5
347	G116	7011	319.5
348	G114	6995	202.5
349	G112	6979	319.5
350	G110	6963	202.5
351	G108	6947	319.5
352	G106	6931	202.5
353	G104	6915	319.5
354	G102	6899	202.5
355	G100	6883	319.5
356	G98	6867	202.5
357	G96	6851	319.5
358	G94	6835	202.5
359	G92	6819	319.5
360	G90	6803	202.5
361	G88	6787	319.5
362	G86	6771	202.5
363	G84	6755	319.5
364	G82	6739	202.5
365	G80	6723	319.5
366	G78	6707	202.5
367	G76	6691	319.5
368	G74	6675	202.5
369	G72	6659	319.5
370	G70	6643	202.5
371	G68	6627	319.5
372	G66	6611	202.5
373	G64	6595	319.5
374	G62	6579	202.5
375	G60	6563	319.5
376	G58	6547	202.5
377	G56	6531	319.5
378	G54	6515	202.5
379	G52	6499	319.5
380	G50	6483	202.5
381	G48	6467	319.5
382	G46	6451	202.5
383	G44	6435	319.5
384	G42	6419	202.5
385	G40	6403	319.5
386	G38	6387	202.5
387	G36	6371	319.5
388	G34	6355	202.5
389	G32	6339	319.5
390	G30	6323	202.5
391	G28	6307	319.5
392	G26	6291	202.5
393	G24	6275	319.5
394	G22	6259	202.5
395	G20	6243	319.5
396	G18	6227	202.5
397	G16	6211	319.5
398	G14	6195	202.5
399	G12	6179	319.5
400	G10	6163	202.5
401	G8	6147	319.5
402	G6	6131	202.5
403	G4	6115	319.5
404	G2	6099	202.5
405	DUMMY21	6083	319.5
406	DUMMY22	6047	319.5
407	S720	6031	202.5
408	S719	6015	319.5
409	S718	5999	202.5
410	S717	5983	319.5
411	S716	5967	202.5
412	S715	5951	319.5
413	S714	5935	202.5
414	S713	5919	319.5
415	S712	5903	202.5
416	S711	5887	319.5
417	S710	5871	202.5
418	S709	5855	319.5
419	S708	5839	202.5
420	S707	5823	319.5
421	S706	5807	202.5
422	S705	5791	319.5
423	S704	5775	202.5
424	S703	5759	319.5
425	S702	5743	202.5
426	S701	5727	319.5
427	S700	5711	202.5
428	S699	5695	319.5
429	S698	5679	202.5
430	S697	5663	319.5
431	S696	5647	202.5
432	S695	5631	319.5
433	S694	5615	202.5
434	S693	5599	319.5
435	S692	5583	202.5
436	S691	5567	319.5
437	S690	5551	202.5
438	S689	5535	319.5
439	S688	5519	202.5
440	S687	5503	319.5
441	S686	5487	202.5

No.	Pad Name	X	Y
442	S685	5471	319.5
443	S684	5455	202.5
444	S683	5439	319.5
445	S682	5423	202.5
446	S681	5407	319.5
447	S680	5391	202.5
448	S679	5375	319.5
449	S678	5359	202.5
450	S677	5343	319.5
451	S676	5327	202.5
452	S675	5311	319.5
453	S674	5295	202.5
454	S673	5279	319.5
455	S672	5263	202.5
456	S671	5247	319.5
457	S670	5231	202.5
458	S669	5215	319.5
459	S668	5199	202.5
460	S667	5183	319.5
461	S666	5167	202.5
462	S665	5151	319.5
463	S664	5135	202.5
464	S663	5119	319.5
465	S662	5103	202.5
466	S661	5087	319.5
467	S660	5071	202.5
468	S659	5055	319.5
469	S658	5039	202.5
470	S657	5023	319.5
471	S656	5007	202.5
472	S655	4991	319.5
473	S654	4975	202.5
474	S653	4959	319.5
475	S652	4943	202.5
476	S651	4927	319.5
477	S650	4911	202.5
478	S649	4895	319.5
479	S648	4879	202.5
480	S647	4863	319.5
481	S646	4847	202.5
482	S645	4831	319.5
483	S644	4815	202.5
484	S643	4799	319.5
485	S642	4783	202.5
486	S641	4767	319.5
487	S640	4751	202.5
488	S639	4735	319.5
489	S638	4719	202.5
490	S637	4703	319.5
491	S636	4687	202.5
492	S635	4671	319.5
493	S634	4655	202.5
494	S633	4639	319.5
495	S632	4623	202.5
496	S631	4607	319.5
497	S630	4591	202.5
498	S629	4575	319.5
499	S628	4559	202.5
500	S627	4543	319.5
501	S626	4527	202.5
502	S625	4511	319.5
503	S624	4495	202.5
504	S623	4479	319.5
505	S622	4463	202.5
506	S621	4447	319.5
507	S620	4431	202.5
508	S619	4415	319.5
509	S618	4399	202.5
510	S617	4383	319.5
511	S616	4367	202.5
512	S615	4351	319.5
513	S614	4335	202.5
514	S613	4319	319.5
515	S612	4303	202.5
516	S611	4287	319.5
517	S610	4271	202.5
518	S609	4255	319.5
519	S608	4239	202.5
520	S607	4223	319.5
521	S606	4207	202.5
522	S605	4191	319.5
523	S604	4175	202.5
524	S603	4159	319.5
525	S602	4143	202.5
526	S601	4127	319.5
527	S600	4111	202.5
528	S599	4095	319.5
529	S598	4079	202.5
530	S597	4063	319.5
531	S596	4047	202.5
532	S595	4031	319.5
533	S594	4015	202.5
534	S593	3999	319.5
535	S592	3983	202.5
536	S591	3967	319.5
537	S590	3951	202.5
538	S589	3935	319.5
539	S588	3919	202.5
540	S587	3903	319.5
541	S586	3887	202.5
542	S585	3871	319.5
543	S584	3855	202.5
544	S583	3839	319.5
545	S582	3823	202.5
546	S581	3807	319.5
547	S580	3791	202.5
548	S579	3775	319.5
549	S578	3759	202.5
550	S577	3743	319.5
551	S576	3727	202.5
552	S575	3711	319.5
553	S574	3695	202.5
554	S573	3679	319.5
555	S572	3663	202.5
556	S571	3647	319.5
557	S570	3631	202.5
558	S569	3615	319.5
559	S568	3599	202.5
560	S567	3583	319.5
561	S566	3567	202.5
562	S565	3551	319.5
563	S564	3535	202.5
564	S563	3519	319.5
565	S562	3503	202.5
566	S561	3487	319.5
567	S560	3471	202.5
568	S559	3455	319.5
569	S558	3439	202.5
570	S557	3423	319.5
571	S556	3407	202.5
572	S555	3391	319.5
573	S554	3375	202.5
574	S553	3359	319.5
575	S552	3343	202.5
576	S551	3327	319.5
577	S550	3311	202.5
578	S549	3295	319.5
579	S548	3279	202.5
580	S547	3263	319.5
581	S546	3247	202.5
582	S545	3231	319.5
583	S544	3215	202.5
584	S543	3199	319.5
585	S542	3183	202.5
586	S541	3167	319.5
587	S540	3151	202.5
588	S539	3135	319.5
589	S538	3119	202.5
590	S537	3103	319.5
591	S536	3087	202.5
592	S535	3071	319.5
593	S534	3055	202.5
594	S533	3039	319.5
595	S532	3023	202.5
596	S531	3007	319.5
597	S530	2991	202.5
598	S529	2975	319.5
599	S528	2959	202.5
600	S527	2943	319.5
601	S526	2927	202.5
602	S525	2911	319.5
603	S524	2895	202.5
604	S523	2879	319.5
605	S522	2863	202.5
606	S521	2847	319.5

No.	Pad Name	X	Y
607	S520	2831	202.5
608	S519	2815	319.5
609	S518	2799	202.5
610	S517	2783	319.5
611	S516	2767	202.5
612	S515	2751	319.5
613	S514	2735	202.5
614	S513	2719	319.5
615	S512	2703	202.5
616	S511	2687	319.5
617	S510	2671	202.5
618	S509	2655	319.5
619	S508	2639	202.5
620	S507	2623	319.5
621	S506	2607	202.5
622	S505	2591	319.5
623	S504	2575	202.5
624	S503	2559	319.5
625	S502	2543	202.5
626	S501	2527	319.5
627	S500	2511	202.5
628	S499	2495	319.5
629	S498	2479	202.5
630	S497	2463	319.5
631	S496	2447	202.5
632	S495	2431	319.5
633	S494	2415	202.5
634	S493	2399	319.5
635	S492	2383	202.5
636	S491	2367	319.5
637	S490	2351	202.5
638	S489	2335	319.5
639	S488	2319	202.5
640	S487	2303	319.5
641	S486	2287	202.5
642	S485	2271	319.5
643	S484	2255	202.5
644	S483	2239	319.5
645	S482	2223	202.5
646	S481	2207	319.5
647	S480	2191	202.5
648	S479	2175	319.5
649	S478	2159	202.5
650	S477	2143	319.5
651	S476	2127	202.5
652	S475	2111	319.5
653	S474	2095	202.5
654	S473	2079	319.5
655	S472	2063	202.5
656	S471	2047	319.5
657	S470	2031	202.5
658	S469	2015	319.5
659	S468	1999	202.5
660	S467	1983	319.5
661	S466	1967	202.5

No.	Pad Name	X	Y
662	S465	1951	319.5
663	S464	1935	202.5
664	S463	1919	319.5
665	S462	1903	202.5
666	S461	1887	319.5
667	S460	1871	202.5
668	S459	1855	319.5
669	S458	1839	202.5
670	S457	1823	319.5
671	S456	1807	202.5
672	S455	1791	319.5
673	S454	1775	202.5
674	S453	1759	319.5
675	S452	1743	202.5
676	S451	1727	319.5
677	S450	1711	202.5
678	S449	1695	319.5
679	S448	1679	202.5
680	S447	1663	319.5
681	S446	1647	202.5
682	S445	1631	319.5
683	S444	1615	202.5
684	S443	1599	319.5
685	S442	1583	202.5
686	S441	1567	319.5
687	S440	1551	202.5
688	S439	1535	319.5
689	S438	1519	202.5
690	S437	1503	319.5
691	S436	1487	202.5
692	S435	1471	319.5
693	S434	1455	202.5
694	S433	1439	319.5
695	S432	1423	202.5
696	S431	1407	319.5
697	S430	1391	202.5
698	S429	1375	319.5
699	S428	1359	202.5
700	S427	1343	319.5
701	S426	1327	202.5
702	S425	1311	319.5
703	S424	1295	202.5
704	S423	1279	319.5
705	S422	1263	202.5
706	S421	1247	319.5
707	S420	1231	202.5
708	S419	1215	319.5
709	S418	1199	202.5
710	S417	1183	319.5
711	S416	1167	202.5
712	S415	1151	319.5
713	S414	1135	202.5
714	S413	1119	319.5
715	S412	1103	202.5
716	S411	1087	319.5

No.	Pad Name	X	Y
717	S410	1071	202.5
718	S409	1055	319.5
719	S408	1039	202.5
720	S407	1023	319.5
721	S406	1007	202.5
722	S405	991	319.5
723	S404	975	202.5
724	S403	959	319.5
725	S402	943	202.5
726	S401	927	319.5
727	S400	911	202.5
728	S399	895	319.5
729	S398	879	202.5
730	S397	863	319.5
731	S396	847	202.5
732	S395	831	319.5
733	S394	815	202.5
734	S393	799	319.5
735	S392	783	202.5
736	S391	767	319.5
737	S390	751	202.5
738	S389	735	319.5
739	S388	719	202.5
740	S387	703	319.5
741	S386	687	202.5
742	S385	671	319.5
743	S384	655	202.5
744	S383	639	319.5
745	S382	623	202.5
746	S381	607	319.5
747	S380	591	202.5
748	S379	575	319.5
749	S378	559	202.5
750	S377	543	319.5
751	S376	527	202.5
752	S375	511	319.5
753	S374	495	202.5
754	S373	479	319.5
755	S372	463	202.5
756	S371	447	319.5
757	S370	431	202.5
758	S369	415	319.5
759	S368	399	202.5
760	S367	383	319.5
761	S366	367	202.5
762	S365	351	319.5
763	S364	335	202.5
764	S363	319	319.5
765	S362	303	202.5
766	S361	287	319.5
767	DUMMY23	271	202.5
768	DUMMY24	-271	202.5
769	S360	-287	319.5
770	S359	-303	202.5
771	S358	-319	319.5

No.	Pad Name	X	Y
772	S357	-335	202.5
773	S356	-351	319.5
774	S355	-367	202.5
775	S354	-383	319.5
776	S353	-399	202.5
777	S352	-415	319.5
778	S351	-431	202.5
779	S350	-447	319.5
780	S349	-463	202.5
781	S348	-479	319.5
782	S347	-495	202.5
783	S346	-511	319.5
784	S345	-527	202.5
785	S344	-543	319.5
786	S343	-559	202.5
787	S342	-575	319.5
788	S341	-591	202.5
789	S340	-607	319.5
790	S339	-623	202.5
791	S338	-639	319.5
792	S337	-655	202.5
793	S336	-671	319.5
794	S335	-687	202.5
795	S334	-703	319.5
796	S333	-719	202.5
797	S332	-735	319.5
798	S331	-751	202.5
799	S330	-767	319.5
800	S329	-783	202.5
801	S328	-799	319.5
802	S327	-815	202.5
803	S326	-831	319.5
804	S325	-847	202.5
805	S324	-863	319.5
806	S323	-879	202.5
807	S322	-895	319.5
808	S321	-911	202.5
809	S320	-927	319.5
810	S319	-943	202.5
811	S318	-959	319.5
812	S317	-975	202.5
813	S316	-991	319.5
814	S315	-1007	202.5
815	S314	-1023	319.5
816	S313	-1039	202.5
817	S312	-1055	319.5
818	S311	-1071	202.5
819	S310	-1087	319.5
820	S309	-1103	202.5
821	S308	-1119	319.5
822	S307	-1135	202.5
823	S306	-1151	319.5
824	S305	-1167	202.5
825	S304	-1183	319.5
826	S303	-1199	202.5
827	S302	-1215	319.5
828	S301	-1231	202.5
829	S300	-1247	319.5
830	S299	-1263	202.5
831	S298	-1279	319.5
832	S297	-1295	202.5
833	S296	-1311	319.5
834	S295	-1327	202.5
835	S294	-1343	319.5
836	S293	-1359	202.5
837	S292	-1375	319.5
838	S291	-1391	202.5
839	S290	-1407	319.5
840	S289	-1423	202.5
841	S288	-1439	319.5
842	S287	-1455	202.5
843	S286	-1471	319.5
844	S285	-1487	202.5
845	S284	-1503	319.5
846	S283	-1519	202.5
847	S282	-1535	319.5
848	S281	-1551	202.5
849	S280	-1567	319.5
850	S279	-1583	202.5
851	S278	-1599	319.5
852	S277	-1615	202.5
853	S276	-1631	319.5
854	S275	-1647	202.5
855	S274	-1663	319.5
856	S273	-1679	202.5
857	S272	-1695	319.5
858	S271	-1711	202.5
859	S270	-1727	319.5
860	S269	-1743	202.5
861	S268	-1759	319.5
862	S267	-1775	202.5
863	S266	-1791	319.5
864	S265	-1807	202.5
865	S264	-1823	319.5
866	S263	-1839	202.5
867	S262	-1855	319.5
868	S261	-1871	202.5
869	S260	-1887	319.5
870	S259	-1903	202.5
871	S258	-1919	319.5
872	S257	-1935	202.5
873	S256	-1951	319.5
874	S255	-1967	202.5
875	S254	-1983	319.5
876	S253	-1999	202.5
877	S252	-2015	319.5
878	S251	-2031	202.5
879	S250	-2047	319.5
880	S249	-2063	202.5
881	S248	-2079	319.5
882	S247	-2095	202.5
883	S246	-2111	319.5
884	S245	-2127	202.5
885	S244	-2143	319.5
886	S243	-2159	202.5
887	S242	-2175	319.5
888	S241	-2191	202.5
889	S240	-2207	319.5
890	S239	-2223	202.5
891	S238	-2239	319.5
892	S237	-2255	202.5
893	S236	-2271	319.5
894	S235	-2287	202.5
895	S234	-2303	319.5
896	S233	-2319	202.5
897	S232	-2335	319.5
898	S231	-2351	202.5
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900	S229	-2383	202.5
901	S228	-2399	319.5
902	S227	-2415	202.5
903	S226	-2431	319.5
904	S225	-2447	202.5
905	S224	-2463	319.5
906	S223	-2479	202.5
907	S222	-2495	319.5
908	S221	-2511	202.5
909	S220	-2527	319.5
910	S219	-2543	202.5
911	S218	-2559	319.5
912	S217	-2575	202.5
913	S216	-2591	319.5
914	S215	-2607	202.5
915	S214	-2623	319.5
916	S213	-2639	202.5
917	S212	-2655	319.5
918	S211	-2671	202.5
919	S210	-2687	319.5
920	S209	-2703	202.5
921	S208	-2719	319.5
922	S207	-2735	202.5
923	S206	-2751	319.5
924	S205	-2767	202.5
925	S204	-2783	319.5
926	S203	-2799	202.5
927	S202	-2815	319.5
928	S201	-2831	202.5
929	S200	-2847	319.5
930	S199	-2863	202.5
931	S198	-2879	319.5
932	S197	-2895	202.5
933	S196	-2911	319.5
934	S195	-2927	202.5
935	S194	-2943	319.5
936	S193	-2959	202.5

No.	Pad Name	X	Y
937	S192	-2975	319.5
938	S191	-2991	202.5
939	S190	-3007	319.5
940	S189	-3023	202.5
941	S188	-3039	319.5
942	S187	-3055	202.5
943	S186	-3071	319.5
944	S185	-3087	202.5
945	S184	-3103	319.5
946	S183	-3119	202.5
947	S182	-3135	319.5
948	S181	-3151	202.5
949	S180	-3167	319.5
950	S179	-3183	202.5
951	S178	-3199	319.5
952	S177	-3215	202.5
953	S176	-3231	319.5
954	S175	-3247	202.5
955	S174	-3263	319.5
956	S173	-3279	202.5
957	S172	-3295	319.5
958	S171	-3311	202.5
959	S170	-3327	319.5
960	S169	-3343	202.5
961	S168	-3359	319.5
962	S167	-3375	202.5
963	S166	-3391	319.5
964	S165	-3407	202.5
965	S164	-3423	319.5
966	S163	-3439	202.5
967	S162	-3455	319.5
968	S161	-3471	202.5
969	S160	-3487	319.5
970	S159	-3503	202.5
971	S158	-3519	319.5
972	S157	-3535	202.5
973	S156	-3551	319.5
974	S155	-3567	202.5
975	S154	-3583	319.5
976	S153	-3599	202.5
977	S152	-3615	319.5
978	S151	-3631	202.5
979	S150	-3647	319.5
980	S149	-3663	202.5
981	S148	-3679	319.5
982	S147	-3695	202.5
983	S146	-3711	319.5
984	S145	-3727	202.5
985	S144	-3743	319.5
986	S143	-3759	202.5
987	S142	-3775	319.5
988	S141	-3791	202.5
989	S140	-3807	319.5
990	S139	-3823	202.5
991	S138	-3839	319.5

No.	Pad Name	X	Y
992	S137	-3855	202.5
993	S136	-3871	319.5
994	S135	-3887	202.5
995	S134	-3903	319.5
996	S133	-3919	202.5
997	S132	-3935	319.5
998	S131	-3951	202.5
999	S130	-3967	319.5
1000	S129	-3983	202.5
1001	S128	-3999	319.5
1002	S127	-4015	202.5
1003	S126	-4031	319.5
1004	S125	-4047	202.5
1005	S124	-4063	319.5
1006	S123	-4079	202.5
1007	S122	-4095	319.5
1008	S121	-4111	202.5
1009	S120	-4127	319.5
1010	S119	-4143	202.5
1011	S118	-4159	319.5
1012	S117	-4175	202.5
1013	S116	-4191	319.5
1014	S115	-4207	202.5
1015	S114	-4223	319.5
1016	S113	-4239	202.5
1017	S112	-4255	319.5
1018	S111	-4271	202.5
1019	S110	-4287	319.5
1020	S109	-4303	202.5
1021	S108	-4319	319.5
1022	S107	-4335	202.5
1023	S106	-4351	319.5
1024	S105	-4367	202.5
1025	S104	-4383	319.5
1026	S103	-4399	202.5
1027	S102	-4415	319.5
1028	S101	-4431	202.5
1029	S100	-4447	319.5
1030	S99	-4463	202.5
1031	S98	-4479	319.5
1032	S97	-4495	202.5
1033	S96	-4511	319.5
1034	S95	-4527	202.5
1035	S94	-4543	319.5
1036	S93	-4559	202.5
1037	S92	-4575	319.5
1038	S91	-4591	202.5
1039	S90	-4607	319.5
1040	S89	-4623	202.5
1041	S88	-4639	319.5
1042	S87	-4655	202.5
1043	S86	-4671	319.5
1044	S85	-4687	202.5
1045	S84	-4703	319.5
1046	S83	-4719	202.5

No.	Pad Name	X	Y
1047	S82	-4735	319.5
1048	S81	-4751	202.5
1049	S80	-4767	319.5
1050	S79	-4783	202.5
1051	S78	-4799	319.5
1052	S77	-4815	202.5
1053	S76	-4831	319.5
1054	S75	-4847	202.5
1055	S74	-4863	319.5
1056	S73	-4879	202.5
1057	S72	-4895	319.5
1058	S71	-4911	202.5
1059	S70	-4927	319.5
1060	S69	-4943	202.5
1061	S68	-4959	319.5
1062	S67	-4975	202.5
1063	S66	-4991	319.5
1064	S65	-5007	202.5
1065	S64	-5023	319.5
1066	S63	-5039	202.5
1067	S62	-5055	319.5
1068	S61	-5071	202.5
1069	S60	-5087	319.5
1070	S59	-5103	202.5
1071	S58	-5119	319.5
1072	S57	-5135	202.5
1073	S56	-5151	319.5
1074	S55	-5167	202.5
1075	S54	-5183	319.5
1076	S53	-5199	202.5
1077	S52	-5215	319.5
1078	S51	-5231	202.5
1079	S50	-5247	319.5
1080	S49	-5263	202.5
1081	S48	-5279	319.5
1082	S47	-5295	202.5
1083	S46	-5311	319.5
1084	S45	-5327	202.5
1085	S44	-5343	319.5
1086	S43	-5359	202.5
1087	S42	-5375	319.5
1088	S41	-5391	202.5
1089	S40	-5407	319.5
1090	S39	-5423	202.5
1091	S38	-5439	319.5
1092	S37	-5455	202.5
1093	S36	-5471	319.5
1094	S35	-5487	202.5
1095	S34	-5503	319.5
1096	S33	-5519	202.5
1097	S32	-5535	319.5
1098	S31	-5551	202.5
1099	S30	-5567	319.5
1100	S29	-5583	202.5
1101	S28	-5599	319.5

No.	Pad Name	X	Y
1102	S27	-5615	202.5
1103	S26	-5631	319.5
1104	S25	-5647	202.5
1105	S24	-5663	319.5
1106	S23	-5679	202.5
1107	S22	-5695	319.5
1108	S21	-5711	202.5
1109	S20	-5727	319.5
1110	S19	-5743	202.5
1111	S18	-5759	319.5
1112	S17	-5775	202.5
1113	S16	-5791	319.5
1114	S15	-5807	202.5
1115	S14	-5823	319.5
1116	S13	-5839	202.5
1117	S12	-5855	319.5
1118	S11	-5871	202.5
1119	S10	-5887	319.5
1120	S9	-5903	202.5
1121	S8	-5919	319.5
1122	S7	-5935	202.5
1123	S6	-5951	319.5
1124	S5	-5967	202.5
1125	S4	-5983	319.5
1126	S3	-5999	202.5
1127	S2	-6015	319.5
1128	S1	-6031	202.5
1129	DUMMY25	-6047	319.5
1130	DUMMY26	-6083	319.5
1131	G1	-6099	202.5
1132	G3	-6115	319.5
1133	G5	-6131	202.5
1134	G7	-6147	319.5
1135	G9	-6163	202.5
1136	G11	-6179	319.5
1137	G13	-6195	202.5
1138	G15	-6211	319.5
1139	G17	-6227	202.5
1140	G19	-6243	319.5
1141	G21	-6259	202.5
1142	G23	-6275	319.5
1143	G25	-6291	202.5
1144	G27	-6307	319.5
1145	G29	-6323	202.5
1146	G31	-6339	319.5
1147	G33	-6355	202.5
1148	G35	-6371	319.5
1149	G37	-6387	202.5
1150	G39	-6403	319.5
1151	G41	-6419	202.5
1152	G43	-6435	319.5
1153	G45	-6451	202.5
1154	G47	-6467	319.5
1155	G49	-6483	202.5
1156	G51	-6499	319.5
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1158	G55	-6531	319.5
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1160	G59	-6563	319.5
1161	G61	-6579	202.5
1162	G63	-6595	319.5
1163	G65	-6611	202.5
1164	G67	-6627	319.5
1165	G69	-6643	202.5
1166	G71	-6659	319.5
1167	G73	-6675	202.5
1168	G75	-6691	319.5
1169	G77	-6707	202.5
1170	G79	-6723	319.5
1171	G81	-6739	202.5
1172	G83	-6755	319.5
1173	G85	-6771	202.5
1174	G87	-6787	319.5
1175	G89	-6803	202.5
1176	G91	-6819	319.5
1177	G93	-6835	202.5
1178	G95	-6851	319.5
1179	G97	-6867	202.5
1180	G99	-6883	319.5
1181	G101	-6899	202.5
1182	G103	-6915	319.5
1183	G105	-6931	202.5
1184	G107	-6947	319.5
1185	G109	-6963	202.5
1186	G111	-6979	319.5
1187	G113	-6995	202.5
1188	G115	-7011	319.5
1189	G117	-7027	202.5
1190	G119	-7043	319.5
1191	G121	-7059	202.5
1192	G123	-7075	319.5
1193	G125	-7091	202.5
1194	G127	-7107	319.5
1195	G129	-7123	202.5
1196	G131	-7139	319.5
1197	G133	-7155	202.5
1198	G135	-7171	319.5
1199	G137	-7187	202.5
1200	G139	-7203	319.5
1201	G141	-7219	202.5
1202	G143	-7235	319.5
1203	G145	-7251	202.5
1204	G147	-7267	319.5
1205	G149	-7283	202.5
1206	G151	-7299	319.5
1207	G153	-7315	202.5
1208	G155	-7331	319.5
1209	G157	-7347	202.5
1210	G159	-7363	319.5
1211	G161	-7379	202.5
1212	G163	-7395	319.5
1213	G165	-7411	202.5
1214	G167	-7427	319.5
1215	G169	-7443	202.5
1216	G171	-7459	319.5
1217	G173	-7475	202.5
1218	G175	-7491	319.5
1219	G177	-7507	202.5
1220	G179	-7523	319.5
1221	G181	-7539	202.5
1222	G183	-7555	319.5
1223	G185	-7571	202.5
1224	G187	-7587	319.5
1225	G189	-7603	202.5
1226	G191	-7619	319.5
1227	G193	-7635	202.5
1228	G195	-7651	319.5
1229	G197	-7667	202.5
1230	G199	-7683	319.5
1231	G201	-7699	202.5
1232	G203	-7715	319.5
1233	G205	-7731	202.5
1234	G207	-7747	319.5
1235	G209	-7763	202.5
1236	G211	-7779	319.5
1237	G213	-7795	202.5
1238	G215	-7811	319.5
1239	G217	-7827	202.5
1240	G219	-7843	319.5
1241	G221	-7859	202.5
1242	G223	-7875	319.5
1243	G225	-7891	202.5
1244	G227	-7907	319.5
1245	G229	-7923	202.5
1246	G231	-7939	319.5
1247	G233	-7955	202.5
1248	G235	-7971	319.5
1249	G237	-7987	202.5
1250	G239	-8003	319.5
1251	G241	-8019	202.5
1252	G243	-8035	319.5
1253	G245	-8051	202.5
1254	G247	-8067	319.5
1255	G249	-8083	202.5
1256	G251	-8099	319.5
1257	G253	-8115	202.5
1258	G255	-8131	319.5
1259	G257	-8147	202.5
1260	G259	-8163	319.5
1261	G261	-8179	202.5
1262	G263	-8195	319.5
1263	G265	-8211	202.5
1264	G267	-8227	319.5
1265	G269	-8243	202.5
1266	G271	-8259	319.5

No.	Pad Name	X	Y
1267	G273	-8275	202.5
1268	G275	-8291	319.5
1269	G277	-8307	202.5
1270	G279	-8323	319.5
1271	G281	-8339	202.5
1272	G283	-8355	319.5
1273	G285	-8371	202.5
1274	G287	-8387	319.5
1275	G289	-8403	202.5
1276	G291	-8419	319.5

No.	Pad Name	X	Y
1277	G293	-8435	202.5
1278	G295	-8451	319.5
1279	G297	-8467	202.5
1280	G299	-8483	319.5
1281	G301	-8499	202.5
1282	G303	-8515	319.5
1283	G305	-8531	202.5
1284	G307	-8547	319.5
1285	G309	-8563	202.5
1286	G311	-8579	319.5

No.	Pad Name	X	Y
1287	G313	-8595	202.5
1288	G315	-8611	319.5
1289	G317	-8627	202.5
1290	G319	-8643	319.5
1291	DUMMY27	-8659	202.5

14.5. Alignment Mark

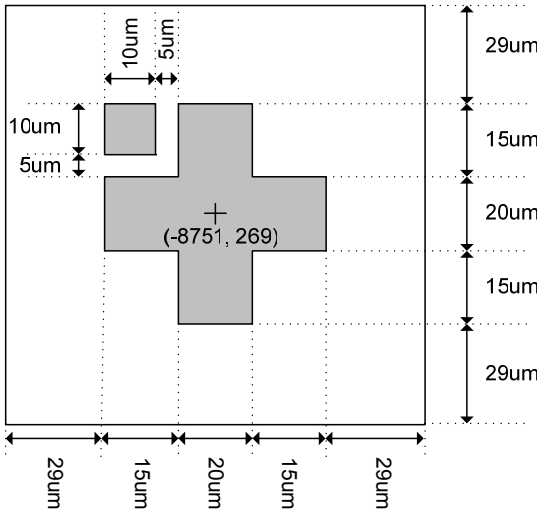
--Alignment Mark coordinate

Left (-8751, 269)

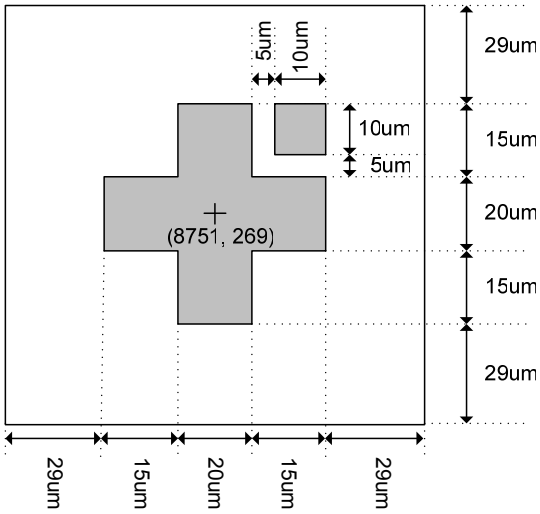
Right (8751, 269)

--Alignment Mark size

Left



Right



15. COG PRODUCTS MANUFACTURING GUIDELINES

15.1. Purpose:

The purpose of this specification is to identify ACF bonding process, so that customers can use properly ACF and Chip during the assembly.

15.2. Scope:

ACF bonding process

15.3. Noun definition

15.3.1. COG: Chip on Glass

15.3.2. ACF (Anisotropic Cunductive Film): .ACF is a functional adhesive tape which is able to connect (conductivity, adhesion, insulation) multiterminals in one time.

15.3.3. CTE: Coefficient of thermal expansion

15.4. Responsibility unity:

ORISETECH Quality Assurance unity

15.5. Contents:

15.5.1. Applicable documents

IPC-SM-782: Surface Mount Design & Land Pattern Standard

IPC-7351Generic Requirements for Surface Mount Design and Land Pattern Standard.

IPC JEDEC: J-STD-033A Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

JESD22-B111: Board Level Drop Test of Components for Handheld Electronic Products

IPC-A-610: Acceptability of Electronic Assemblies

15.5.2. ACF Characteristics:

10.5.2.1 Three factors to achieve the connection: Temperature, Pressure, Time.

15.5.3. ACF process :

10.5.3.1 To use Low Temperature and Low stress ACF is recommended for thin chip as 300 um.

10.5.3.2 Warp issues may happen if customers do not use Low Temperature and Low stress ACF for long chip .And warp issues may induce chip broken after ACF bonding for the CTE mismatch of Glass and ACF and Chip.

10.5.3.3 To use 3um ACF is recommended for BUMP space is less than 13um.

10.5.3.4 To use Low temperature and long time bonding is recommended if delamination happens in edge of chip.

10.5.3.5 For fine pitch and thin chip (300 um) products, customer should review ACF bonding condition with ACF maker.

15.6. References:

*IPC:

http://www.ipc.org

*HDPUG (High Density Package Users Group)

http://www.hdpug.org

*JEDEC (Joint Electronic Device Engineering Council)

http://www.jedec.org

*JEITA (Japan Electronic Industry Association)

http://www.jeita.org

16. DISCLAIMER

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17. REVISION HISTORY

Date	Revision #	Description	Page
Jan. 22, 2009	0.1	Original.	95